SDA-FBDIMM

Software Option

New Compliance Framework

For AMB Point-to-Point Specification (V. 0.85)

Featuring LeCroy's

Operator's Manual

July 2006

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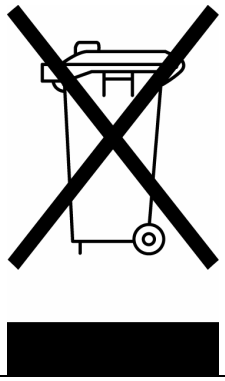

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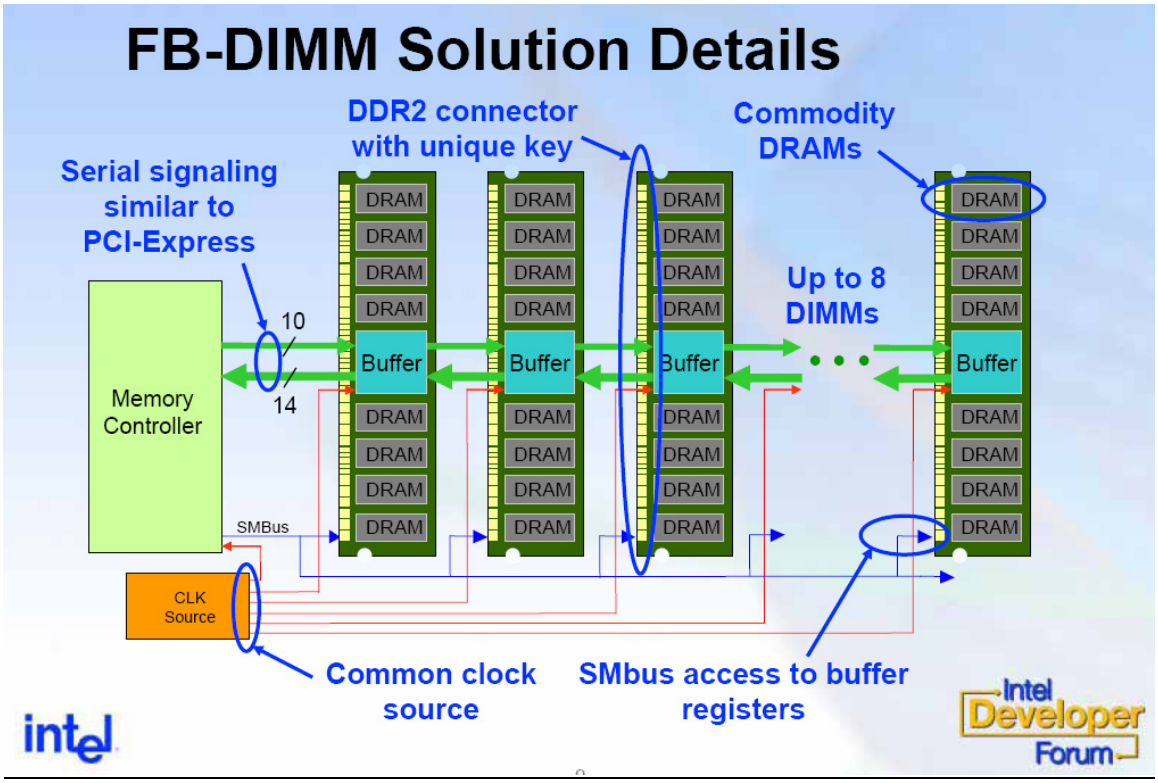
INTRODUCTION TO FB-DIMM

Product Definition and Technology

The FB-DIMM (fully buffered dual in-line memory module) interface is a new memory interface being implemented by the memory industry (spearheaded by Intel) that was created to respond to increasing limitations in channel capacity, occurring with DDR-X (Double Data Rate) implementations. As server performance increases, the traditional stub configuration of standard DRAM has hit a ceiling.

- FB-DIMM buffers the DRAM data pins from the channel and uses point-to-point links to eliminate the stub.
- FB-DIMM capacity scales throughout DDR2 & DDR3 generations.

FB-DIMM Architecture



Each memory module contains a Buffer that interfaces with the AMB (Advanced Memory Buffer) in such a way that data transfers to/from the processor bus are carried out through the AMB interface. The second interface of interest is the point-to-point serial link between the memory modules, all implemented in the same manner and using differential signals with amplitude, timing, and clocking schemes similar to the familiar PCI Express implementation.

The standardization of FB-DIMM specifications is managed through JEDEC Committees 40 and 45.

INTRODUCTION TO SDA-FBDIMM

What is SDA-FBDIMM?

The New LeCroy FB-DIMM Development Software for the SDA 11000 serial data analyzer is designed with two major objectives in mind:

First and foremost, SDA-FBDIMM provides the necessary tools to develop and validate FB-DIMM compliant devices in a systematic, step-by-step fashion, in accordance with the latest standards and specification documents published by JEDEC.

Quick and easy access to all of the compliance test requirements from the AMB Point to Point specifications, and summarized in the X-Replay Automated test Environment. LeCroy enables in-process measurement and reporting of FB-DIMM critical parameters.

The standard features of the SDA also provide a broad toolset for advanced debugging of these interfaces, including jitter, eye pattern, and bit error rate.

The New LeCroy FB-DIMM Development Software (SDA-FBDIMM) is available as an option to the SDA 11000 Serial Data Analyzer by installing version 4.6 or newer of X-Stream scope firmware. SDA-FBDIMM should be used in conjunction with the minimum necessary instrument bandwidth:

- For FB-DIMM running at 3.2 Gb/sec, SDA 6000A / SDA 6020
- For FB-DIMM running at 4.0 and 4.8 Gb/sec, a SDA 11000 or higher BW is necessary.

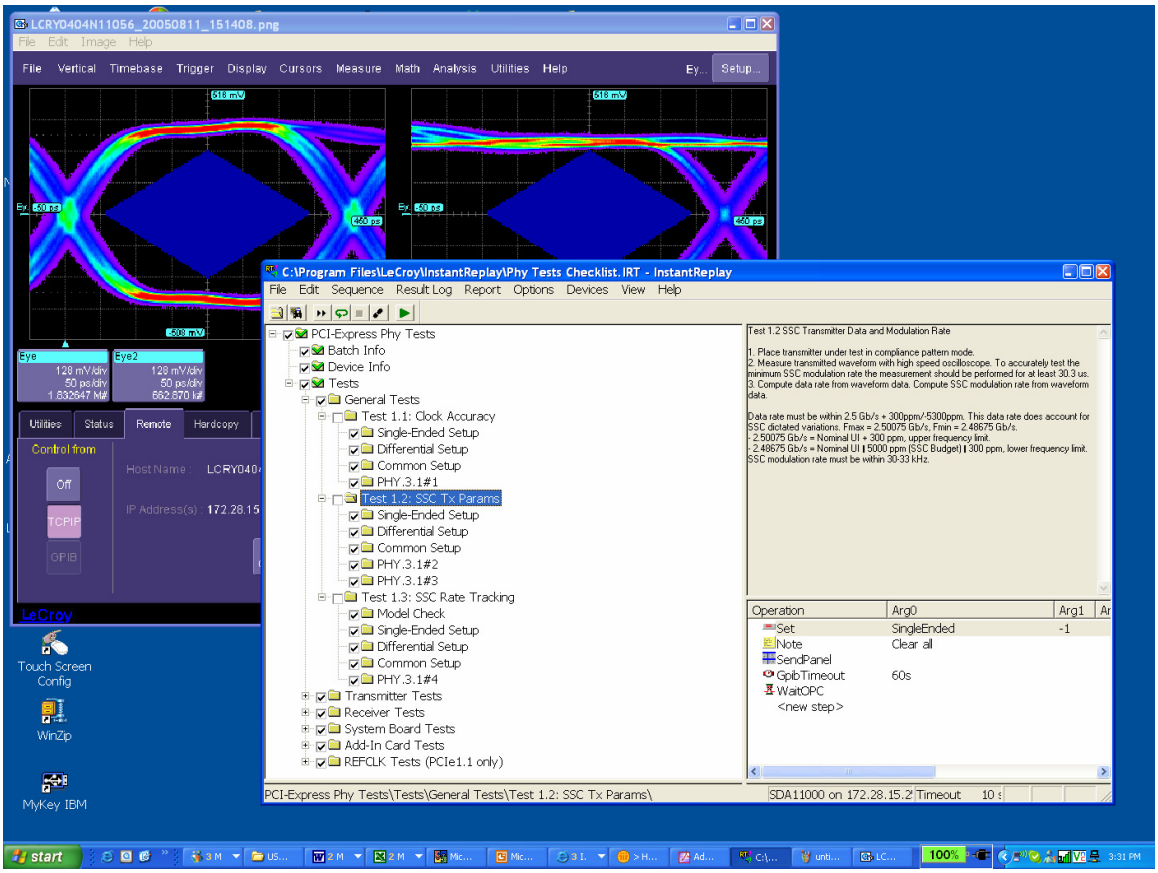
Required Equipment

- SDA 11000 equipped with ASDA-J Advanced Serial Data Analysis software option.
- FB-DIMM Compliance & Development software option (LeCroy SDA-FBDIMM)
- FB-DIMM Parametric test fixture (Agilent N4236A or equivalent) for Transmitter tests
- 2 differential probes (D600-type for SDA6000A or SDA6020, D11000PS-type for SDA 11000)
- FB-DIMM Slot test fixture (Agilent N4238A or equivalent) for Receiver tests
- Channel Test Card (CTC) fixture or Certified Motherboard for Reference Clock tests
- 1 SMA ‘T’ connector
- 1 BNC-to-SMA adapter
- A Host computer, though not required, is highly recommended to execute X-Replay, the Compliance & Development Software Engine.
- Option DMD-1 (Dual Monitor Display), though not required, is highly recommended for execution of X-Replay in a second screen.

What Is X-Replay?

The new FB-DIMM Software application incorporates X-Replay, a unique application framework. X-Replay is an MS Windows-based application that contains all the commands and instructions necessary to configure, acquire, display, and report measurement results. For instance, X-Replay environment enables you to:

- Create or change test criteria in order to make context-sensitive parametric measurements.
- Export all test results as XML (for import into a database program such as Microsoft Access) for further manipulation.
- Generate reports from within X-Replay showing the latest test results. Reports are html (meant to be viewed with Microsoft Internet Explorer) or pdf formatted for Adobe Acrobat users.



The FB-DIMM Compliance software resides in X-Stream scope software in the scope, and it is activated through the use of an alphanumeric code matched to the scope serial number. This code is unique to each scope serial number, and it is activated when ordering SDA-FBDIMM software.

While the software key enables the scope to perform the measurements, X-Replay contains the FB-DIMM script, the test results database and the report generation engine. For ultimate flexibility, X-Replay can be executed from a host computer at a location different from the scope, provided that there is a Windows-compatible network connection. X-Replay comes installed on the scope by default.

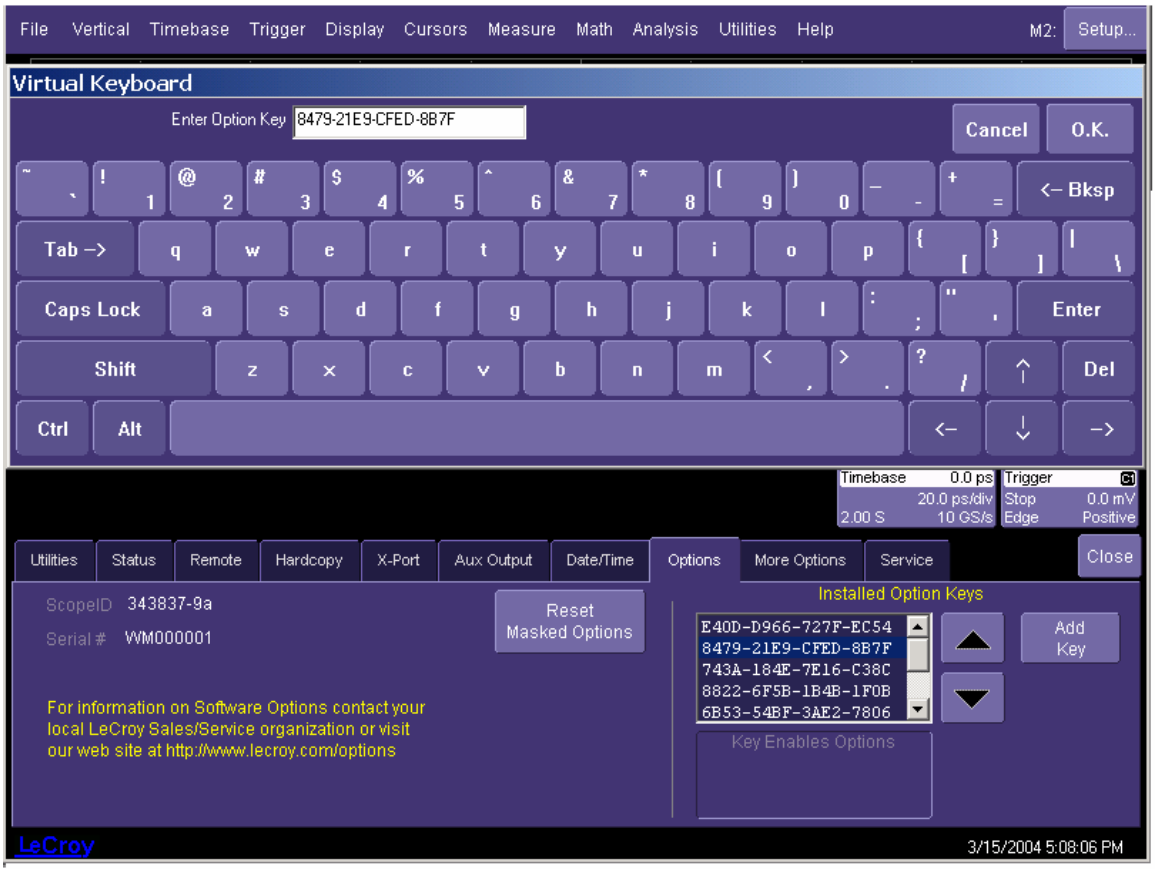
SOFTWARE INSTALLATION AND SYSTEM CONFIGURATION

Option Key Installation

When ordered as an option to a new instrument, no installation is necessary. Installation is, however, required when the option is ordered after the oscilloscope is purchased. An option key will be issued at the time the option is purchased.

To enter the option key code,

1. Touch **Utilities** in the menu bar, then **Utilities Setup…** in the drop-down menu.
2. Select the **Options** tab from the Utilities dialog.
3. In the **Options** dialog, touch the **Add Key** button and enter the option key in the dialog box using the pop-up keyboard.



Entering the option key code for the SDA-FBDIMM software option

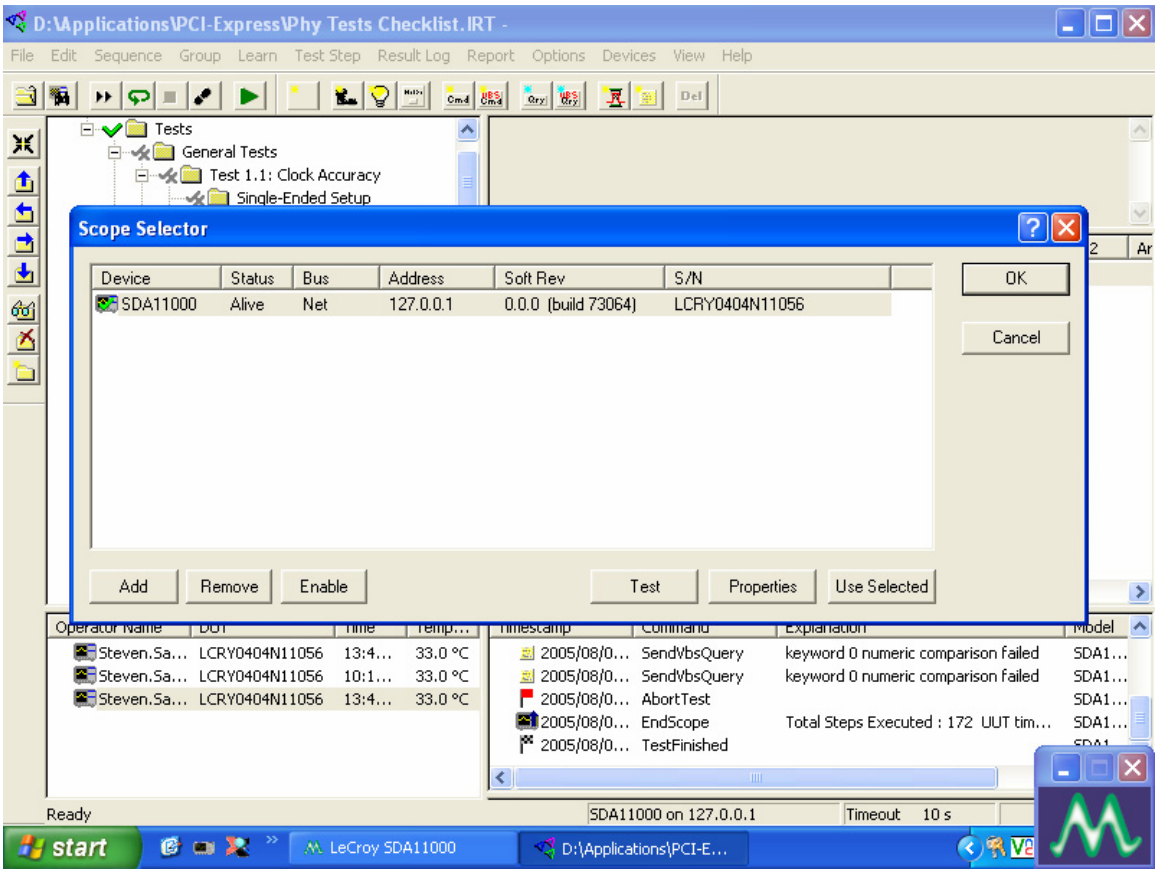
CD-ROM Installation

When ordered as an upgrade to an existing X-Stream oscilloscope, an Application Software CD-ROM is supplied containing X-Replay and other software installation files. Follow the specific instructions in the Installer application. The installation process will prompt you, as required, for specific location of data files and test results, reports, scripts, etc.

Typical (Recommended) Configuration

SDA-FBDIMM software can be executed from the scope PC or from a Host PC. By default, a new scope will come equipped with X-Replay installed in the scope. LeCroy recommends that you run SDA-FBDIMM in a scope equipped with Dual Monitor Display capability (Option DMD-1), such that the waveform and measurements are displayed in the scope LCD display, whereas the X-Replay application and test results are displayed on a second monitor. By default, the scope appears as a local host (IP address is 127.0.0.1) when X-Replay is executed in the scope computer. To verify correct operation, the following steps must be taken once the scope is turned on:

1. Minimize the X-Stream scope window.
2. Run X-Replay.
3. From the menu bar select **Devices**, then **Scope Manager** from the drop-down menu. The scope selector window displays the scope attached (in this case, an SDA 11000).



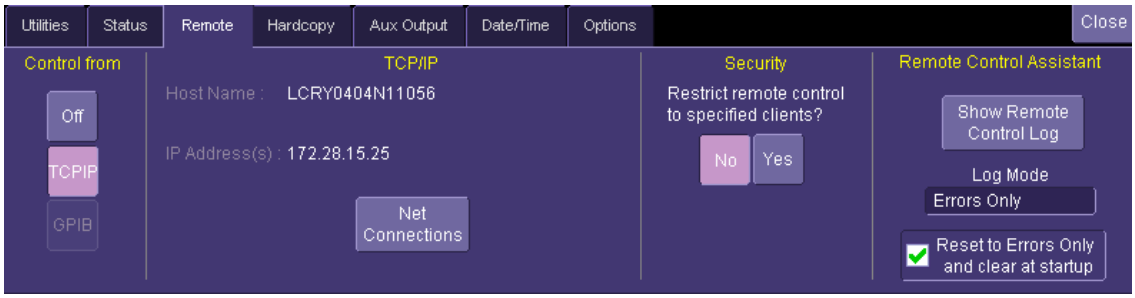
4. Click the **Test** button. If the scope is detected, a message box will indicate that the test is OK. X-Replay is now ready for use.

Remote (Networked) Configuration

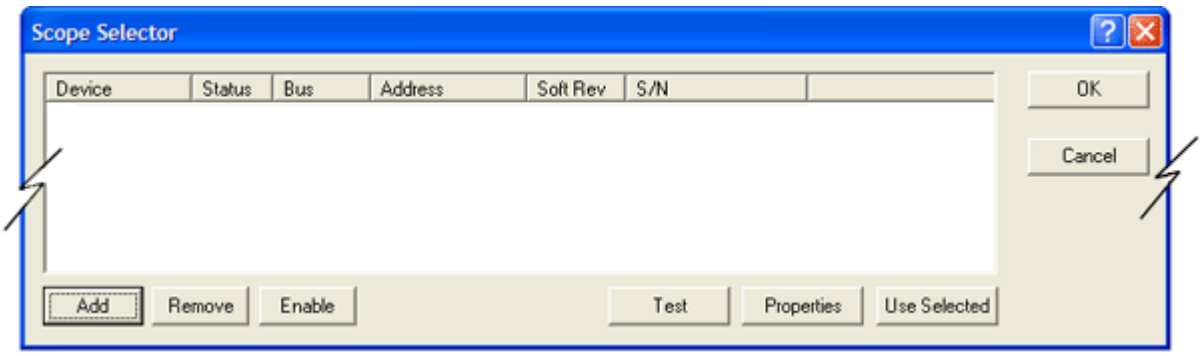
Of course, it is also possible to run SDA-FBDIMM by installing X-Replay in a host PC, controlling the scope via a Windows Network/LAN Connection. This allows you to run other instruments or applications from the host PC (for example, setting up and configuring more than one LeCroy instrument). The scope must already be configured, and an IP address (fixed or network-assigned) must already be established.

As an example of how to set up the scope using X-Replay over a LAN (Local Area Network), follow these steps:

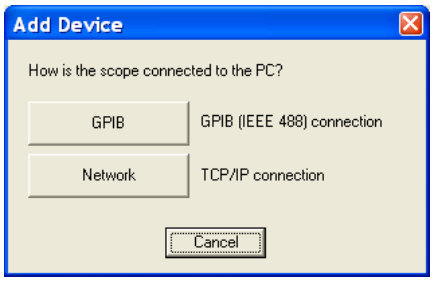
1. Verify in the **Utilities**, **Remote** dialog that the scope has an IP address. Control is set to TCP/IP as shown below.



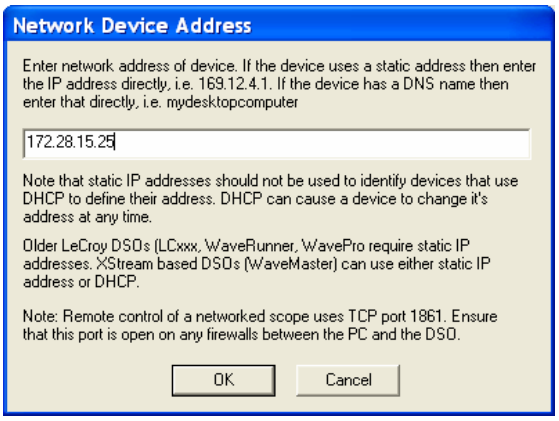
2. Make sure that the host PC is connected to the same LAN as the scope. If unsure, contact your system administrator.
3. Run X-Replay in the host PC and select Devices menu, then scope selector. The screen should have no devices enabled at this time.



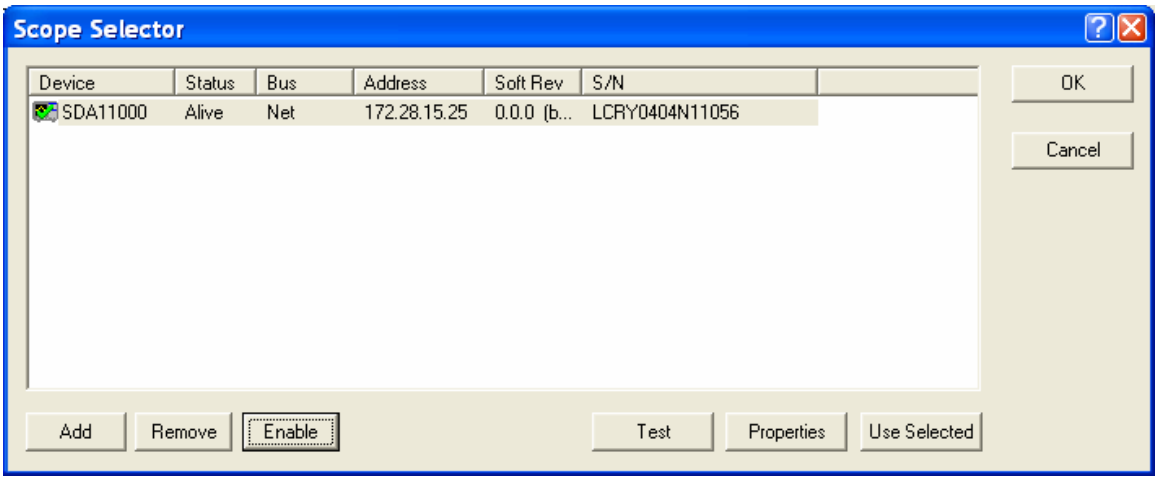
4. Click the **Add** button. Select the connection method (GPIB or Network)



5. Select **Network**, then enter the IP address from step #1



6. Click **OK**. The Scope Selector window displays the information about the scope connected to the LAN. In our example, an SDA 11000 is connected, as shown below:



PREPARING TO MAKE FB-DIMM MEASUREMENTS

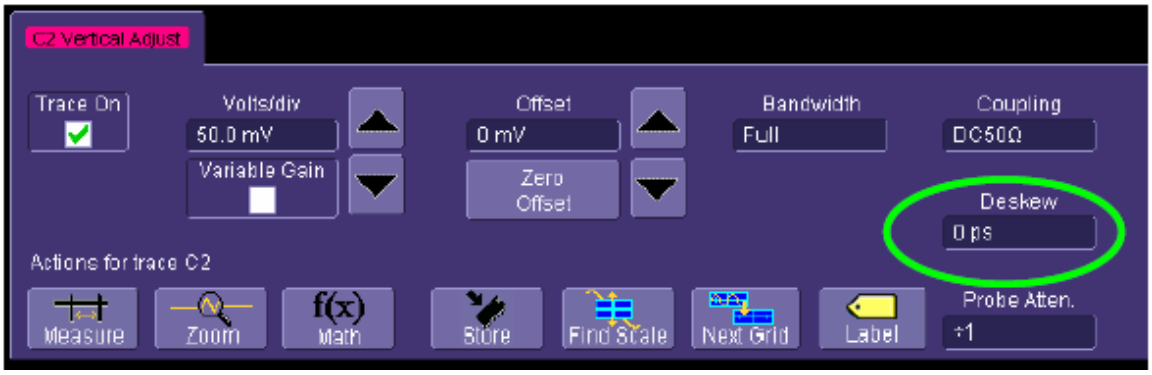
Channel Deskew (SMA Cables)

FB-DIMM signals are properly probed using two separate channels on the oscilloscope, connected to the appropriate SMA jacks on the test fixture. The highest measurement accuracy is achieved when the timing skew between the two channels is calibrated. This is performed using the "Deskew" control on one of the two channels to which the differential signal is connected, as follows:

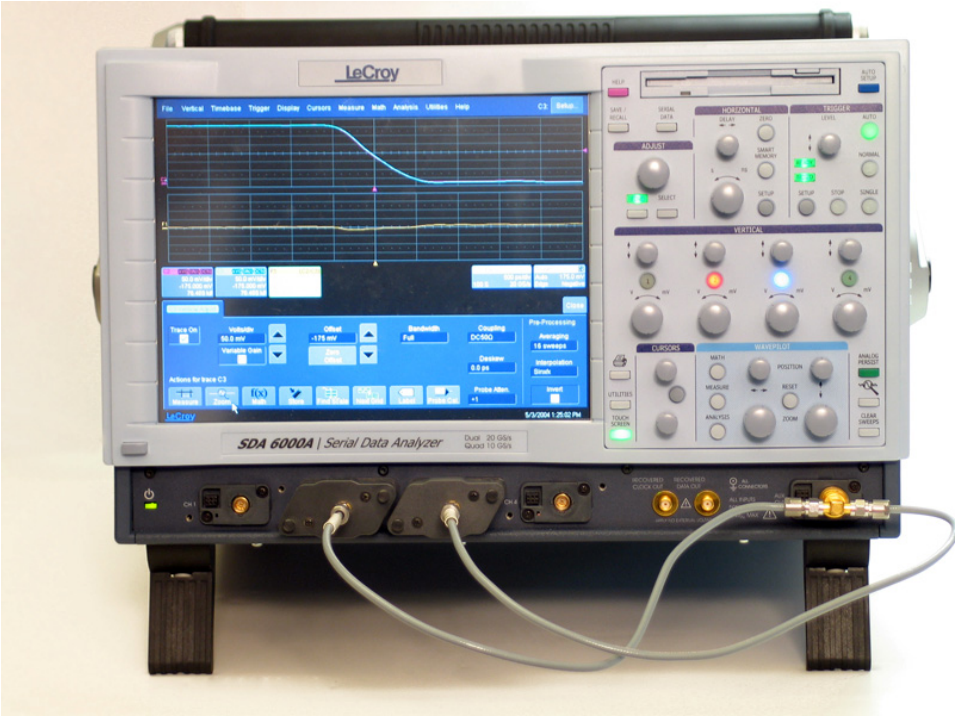
1. Attach the calibrator signal to both input channels, using a T connector, to rout the calibrator signal on the SDA front panel through the same cables that will be connected to the fixture.
2. Set interpolation of both channels to **(Sinx)/x**, using the **Interpolation** control in the "Vertical Adjust" dialog for each channel.
3. Check the **Invert** checkbox on one channel.
4. Create a Difference math waveform by selecting **Math** in the menu bar, then **Math Setup…** in the drop-down menu. Enter the channels to which your signal is connected in the **Source1** and **Source2** fields, and select **Difference** from the **Operator1** menu. The math function is thus defined as the difference between the 2 channels probing the D^+ and D^- signals.
5. While viewing the math trace, adjust the **Deskew** control in one of the channels until the math trace is as flat as possible.

Note: With the **Deskew** control highlighted, you can use the front panel adjust knob to make the adjustment.

The best accuracy is achieved by setting the level of the calibrator signal to match the expected levels of the signal under test, and with the calibrator set to its maximum frequency (5 MHz). The calibrator settings can be found in **Utilities**, **Aux Output** dialog.



Deskew control in channel menu. Adjust this value to achieve minimum skew.

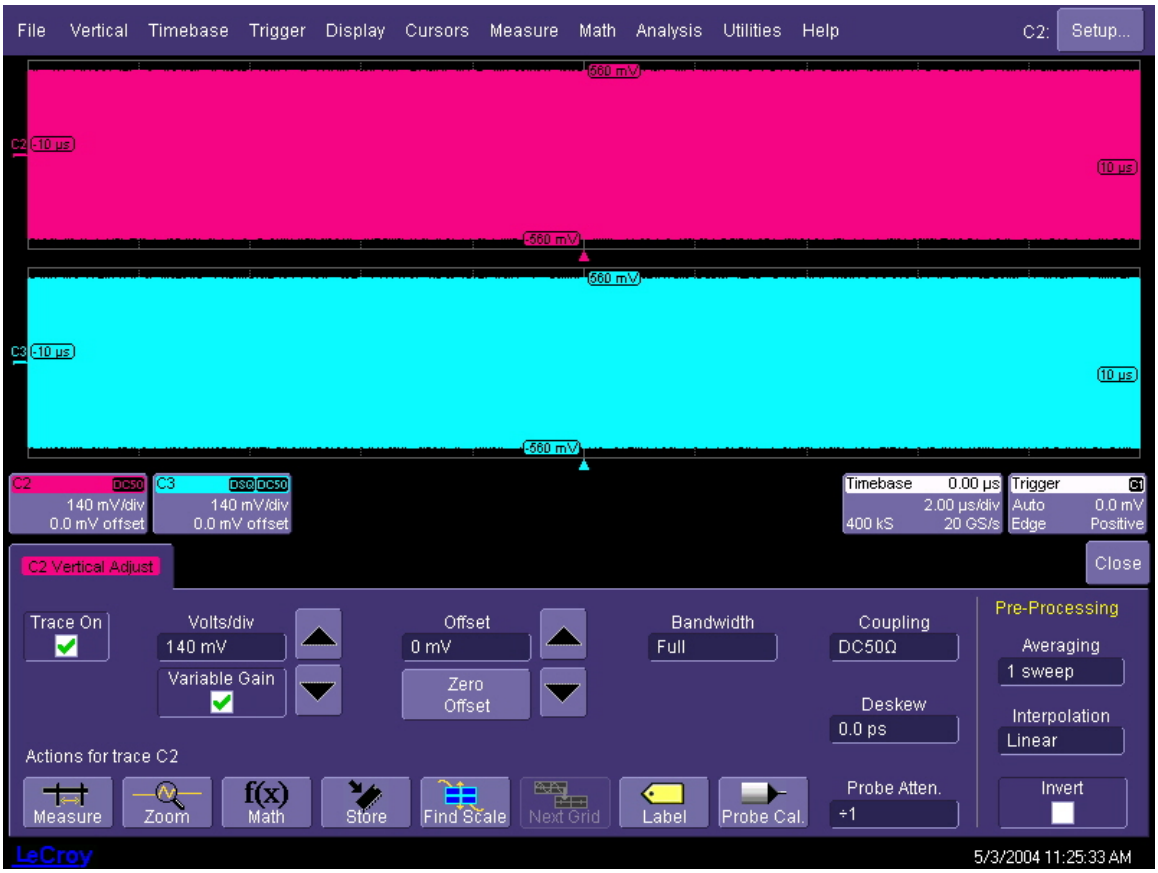


Deskew cable setup. The calibrator signal is connected to the cables using a T connector or resistive divider. The calibrator peak voltage should be set to the same value as the nominal voltage of D+ and D-.

Differential Probe Calibration

The FB-DIMM signal can be applied to a single channel of the SDA using a differential probe; or directly to two channels, using one of the test fixtures described above. In either case, the signal level should be maximized on the instrument to achieve the best overall accuracy. The signal level is set in the “Vertical Adjust” dialog, or by using the front panel knobs. The best peaking can be achieved by checking the **Variable Gain** checkbox, which allows finer gain steps in the control knobs.

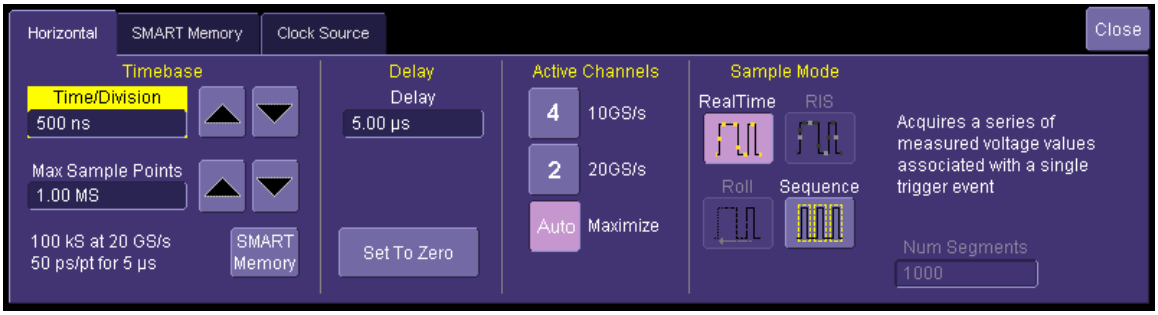
With the introduction of the 40 GS/s, 2 channel, 11 GHz BW (20 GS/s, 4 channel , 6 GHz) scope with Digital Bandwidth Interleaving (DBI), high-speed FB-DIMM measurements (up to 4.8 Gb/s) can now be accomplished. Additionally, the use of two D11000 probes enables the measurement of interlane skew on the DBI-enabled channels.

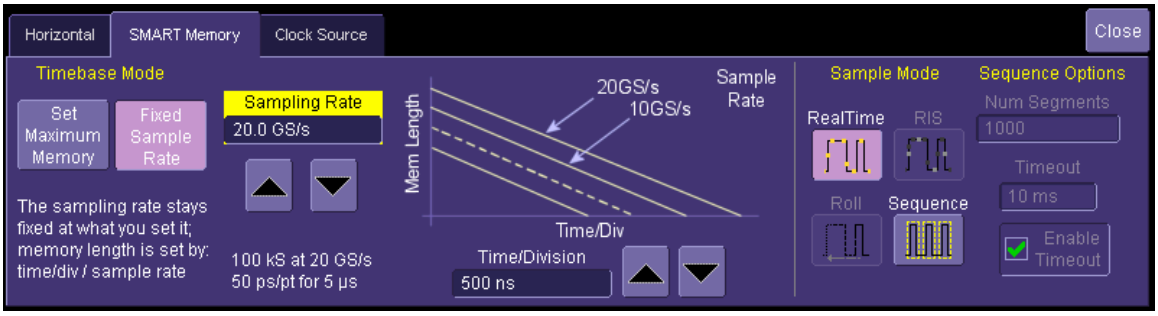


Signals properly adjusted for best accuracy. The signal levels should be adjusted in the "Vertical Adjust" dialog so that at least 6 vertical divisions are filled.

For SDA 6000A (FB-DIMM up to 3.2 Gb/s)

The horizontal scale should be set to a fixed sampling rate of 20 GS/s. This requires that **Auto** or **2** channels be selected in the **Active Channels** control in the **Horizontal** (Timebase) dialog. The record length should be set to a minimum of 8 MS using the **Time/Division** control or the front panel horizontal scale knob. Longer records give more accurate results but also take more time to compute.





Horizontal and memory setup menus properly configured for testing FB-DIMM signals. The maximum (20 GS/s) sampling rate must be used. The SDA 6020 does not have the "Active Channels" control since all channels sample at 20 GS/s.

The signal under test is selected from the **Data Source** menu in the **Serial Data Analysis** main dialog. The source can be any channel, memory, or math trace. If a differential probe is being used to couple the signal to the instrument, the channel to which the probe is attached should be entered into the **Data Source** control. When probing with 2 channels of the instrument attached to a compliance test fixture, a math trace should be defined as the difference between the channel connected to the data+ line and the channel connected to the data- line on the fixture. The channels should be deskewed as described above.

It is also possible to perform measurements on waveform files stored in memory either on the system hard disk or in non-volatile memory. Subtract the memory traces if they are stored as separate (+ and -) waveforms, as described above, or enter the memory into the **Data Source** control directly.

X-REPLAY OPERATION

All the tests covered by this Manual refer to the FB-DIMM High Speed Differential PTP Link at 1.5V Specification, Revision 0.7 (*May 10, 2005)* **JEDEC**

This section covers use of X-Replay and the supplied "FB-DIMM Tests Checklist.irt" script to perform tests described in the PTP document, and generation of a test results report from X-Replay.

X-Replay allows you to test FB-DIMM functionality in several ways:

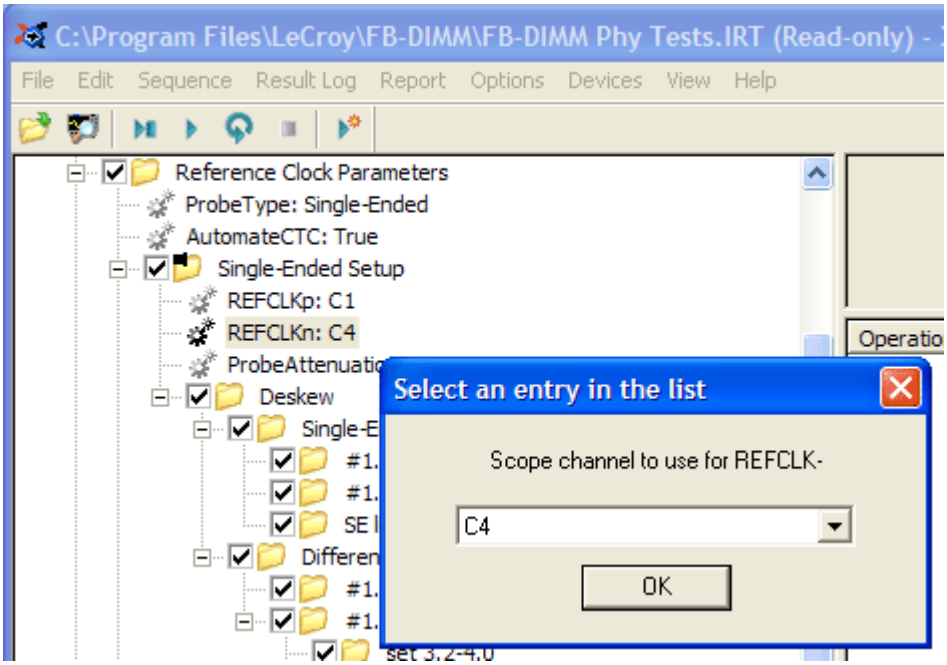
- Select, repeat, and skip tests as required to demonstrate or develop different PHY functions.
- Establish Test Limits for each of the versions of the FB-DIMM specification and modify, create, or delete entire test limit sets.
- Generate Test Reports based on the tests actually run.
- Query the database for test results from prior test sessions or experiment runs.

X-Replay application display is divided into several windows (clockwise, from upper-left):

- Test Sequence Window
- Test Description Window
- Commands Window
- Activity Log Window
- Session Window

Use of Configuration Variables in Test Sequences

Configuration Variables allow you to define system inputs such as signal sources, probe types, specification parameter set to be used for testing, form factors, and other global conditions. These variables can be set prior to beginning tests, or changed between test runs.



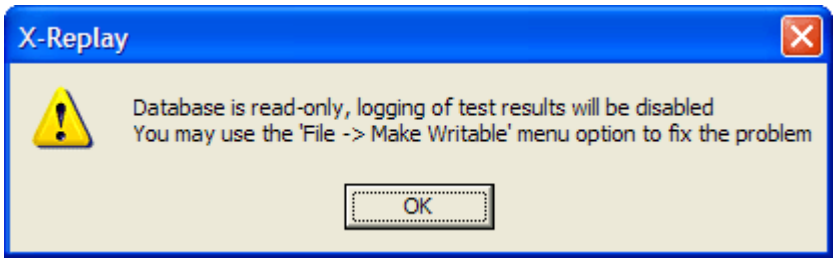
Right-clicking on any variable allows you to reset the variable to its default setting or to change the value to be used for subsequent tests.

Menu Structure

File

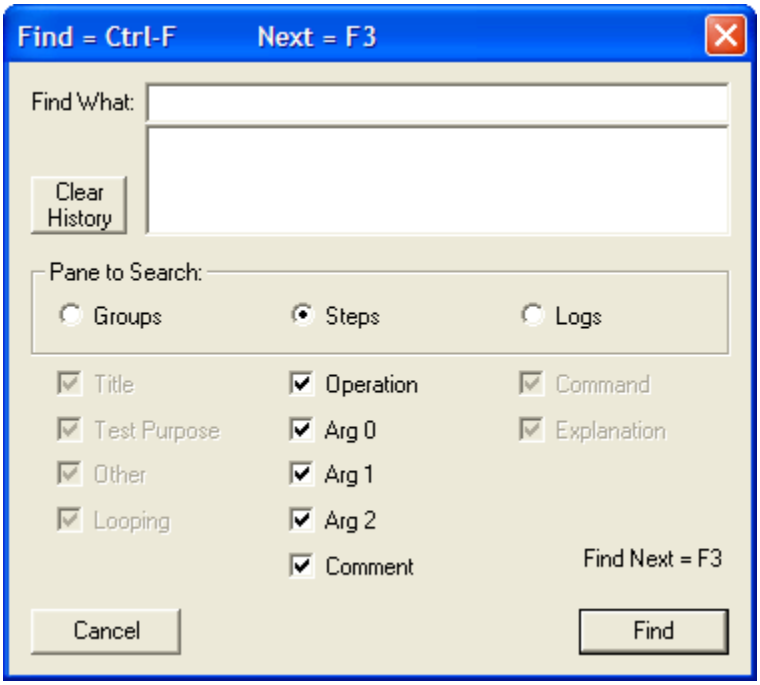
Open Test File (Test Database). The file extension is *.irt

Make Read Only disables writing test results into session log. *Make Writable* reverses the action.



Edit

Performs the Find function to locate specific measurements or actions in the program sequence.



Sequence

Execute program items starting at the designated point. The Menu Toolbar displays the available choices, from left to right:

Open

Search Attached Devices performs a scope search

Single Step [F10] executes one instruction at a time.

Play Selected Group and Children [F5] executes all the checked items in the selected group.

Play Selected Group Continuously executes all checked items in the selected group until *Stop* is selected.

Stop stops execution (active after Play has been selected).

Result Log

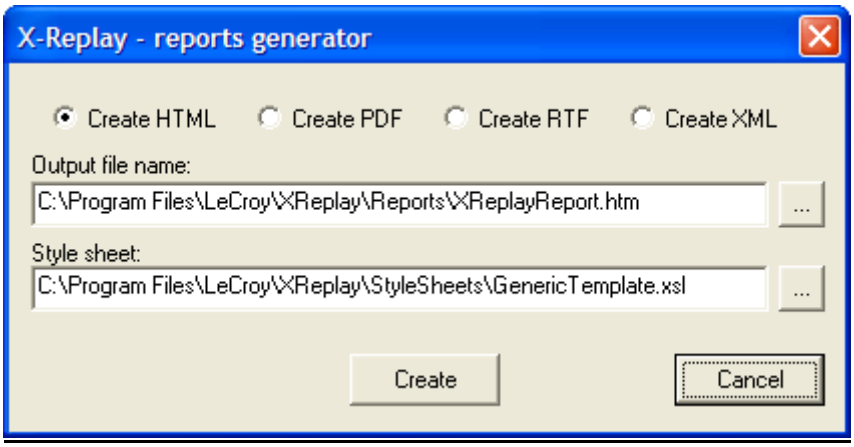
Clear Log removes all the previously recorded activity.

Export to File (ASCII) creates a comma-separated-values set of activity records.

Export to File (ASCII) Standard creates a text file phy tests checklist.logdump.txt.

Report

Creates a report with one of three formats (html, pdf, or rtf) based on the specified report template Style Sheet (*.xsl or *.xslt). For Style sheet, please select the supplied “XReplay_Report.xslt”. The “…” button to the right of the text entry field can be used to browse and find that file. On an SDA, it can be found in D:\Applications\FBDIMM.



Options

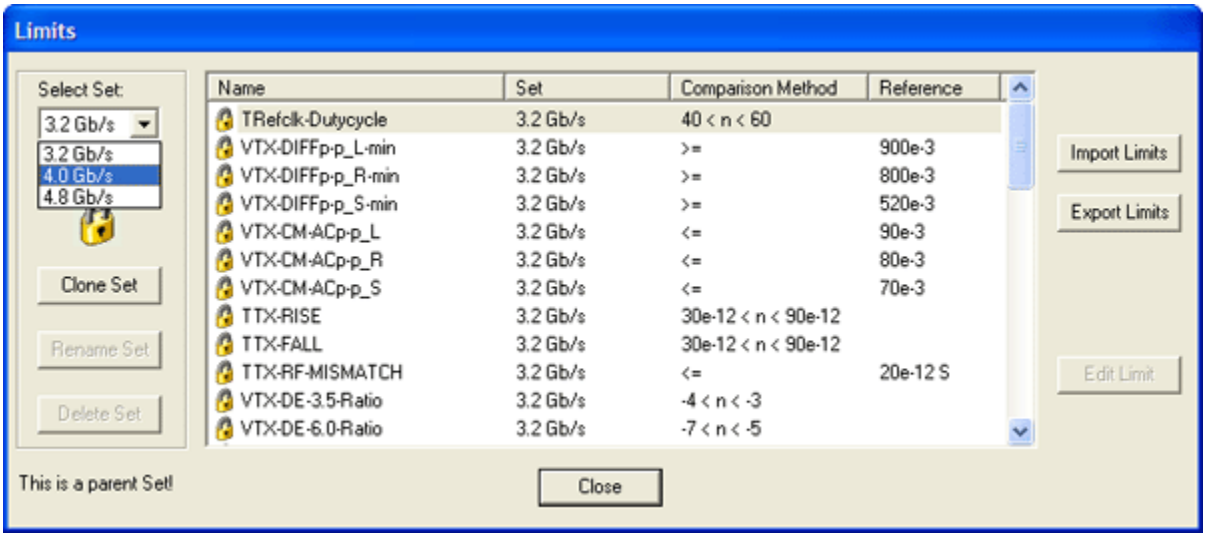
Limits

Select the Limits option to allow the configuration of individual parameters pass/fail criteria; or to edit, rename, and save complete parameter sets.

Clone Set enables you to create a new, named set of limits. Initially, the new set is the same as the set selected when pressing “Clone Set.”

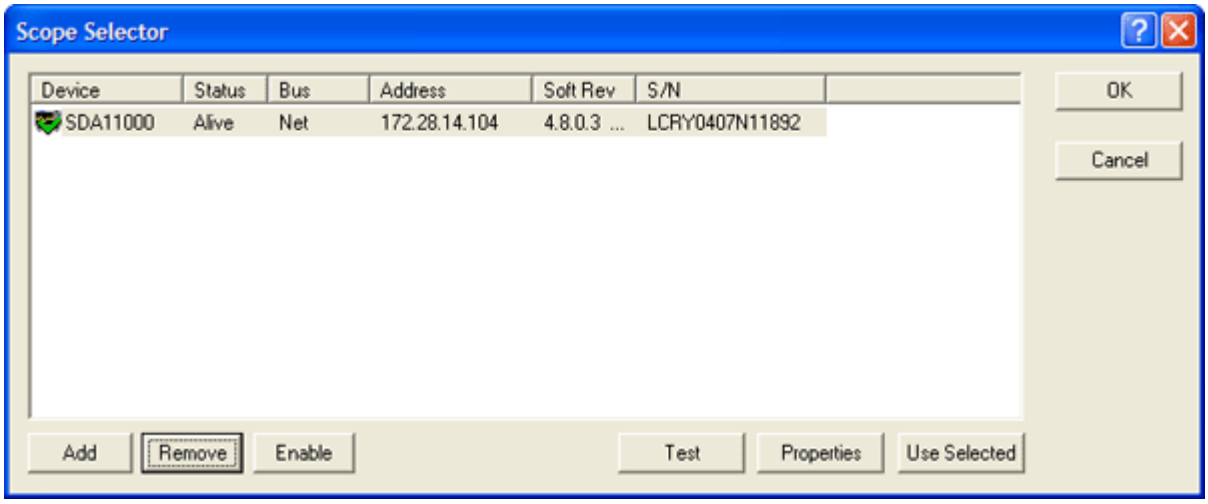
Edit Limit allows limits to be changed to meet specific pass/fail criteria.

Import/Export Limits enables you to transfer entire parameter sets to csv-formatted (MS Excel) files.

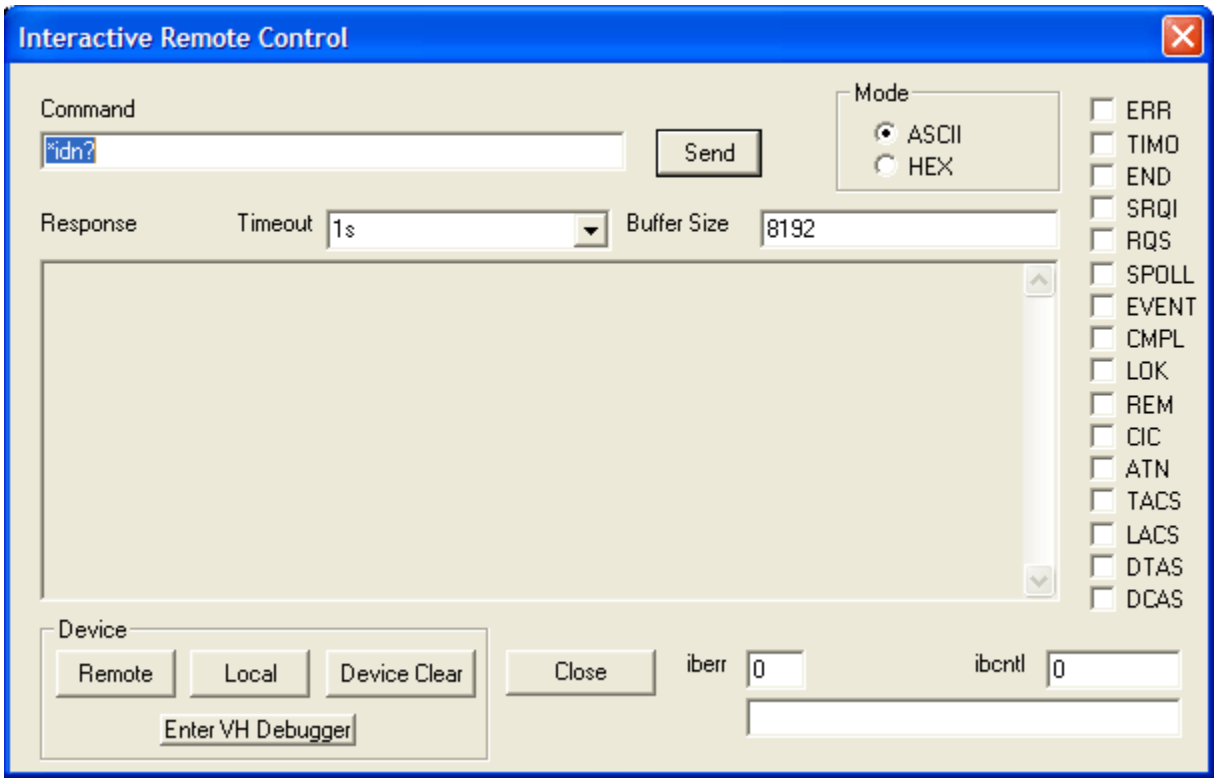


Devices

Scope Manager displays the devices connected to the host computer. There are two supported modes of attaching a device: GPIB or LAN.



Interactive Dialog supports sending and receiving single-line commands to the devices on the list.



View

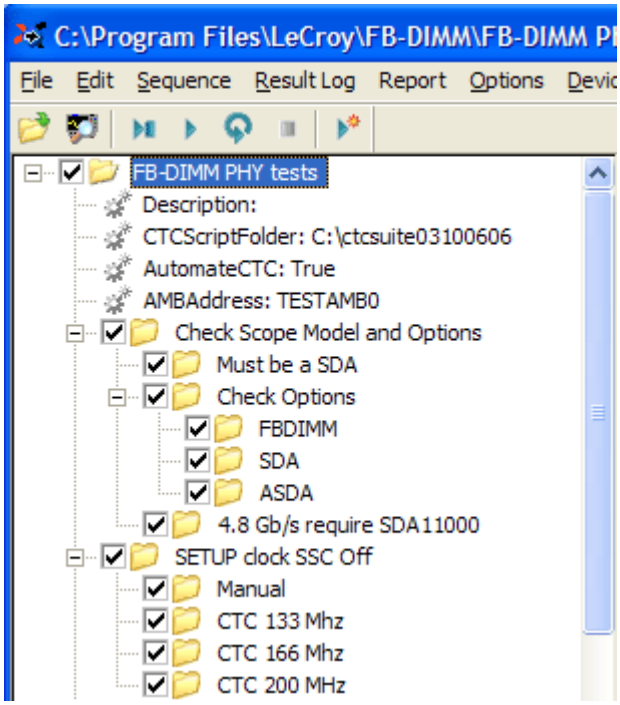
Enables/Disables Toolbar and Status bar

Help

Help Topics

Running FB-DIMM Tests

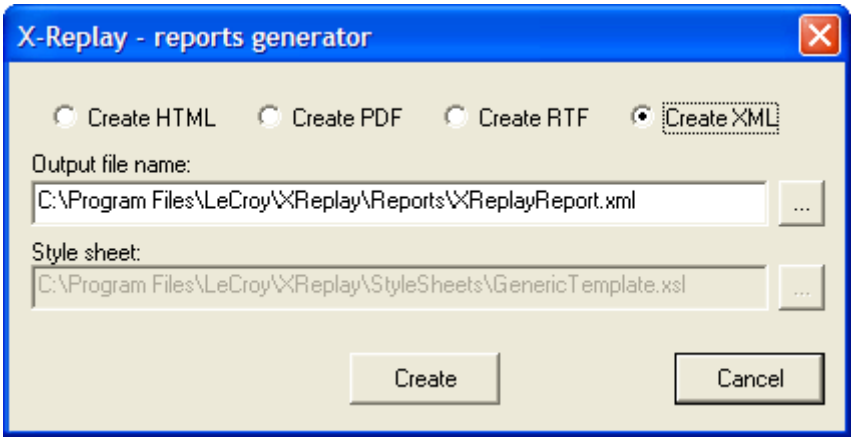
1. Verify proper signal input and observe all deskew and calibration procedures.
2. Run X-Replay application.
3. Open The PHY Tests Checklist database.
4. Select the test groups to be executed.
5. Set up ***Configuration Variables*** as required for the selected tests.
6. Press Play and follow script prompts, as required.



Export to *.XML file – Database Access

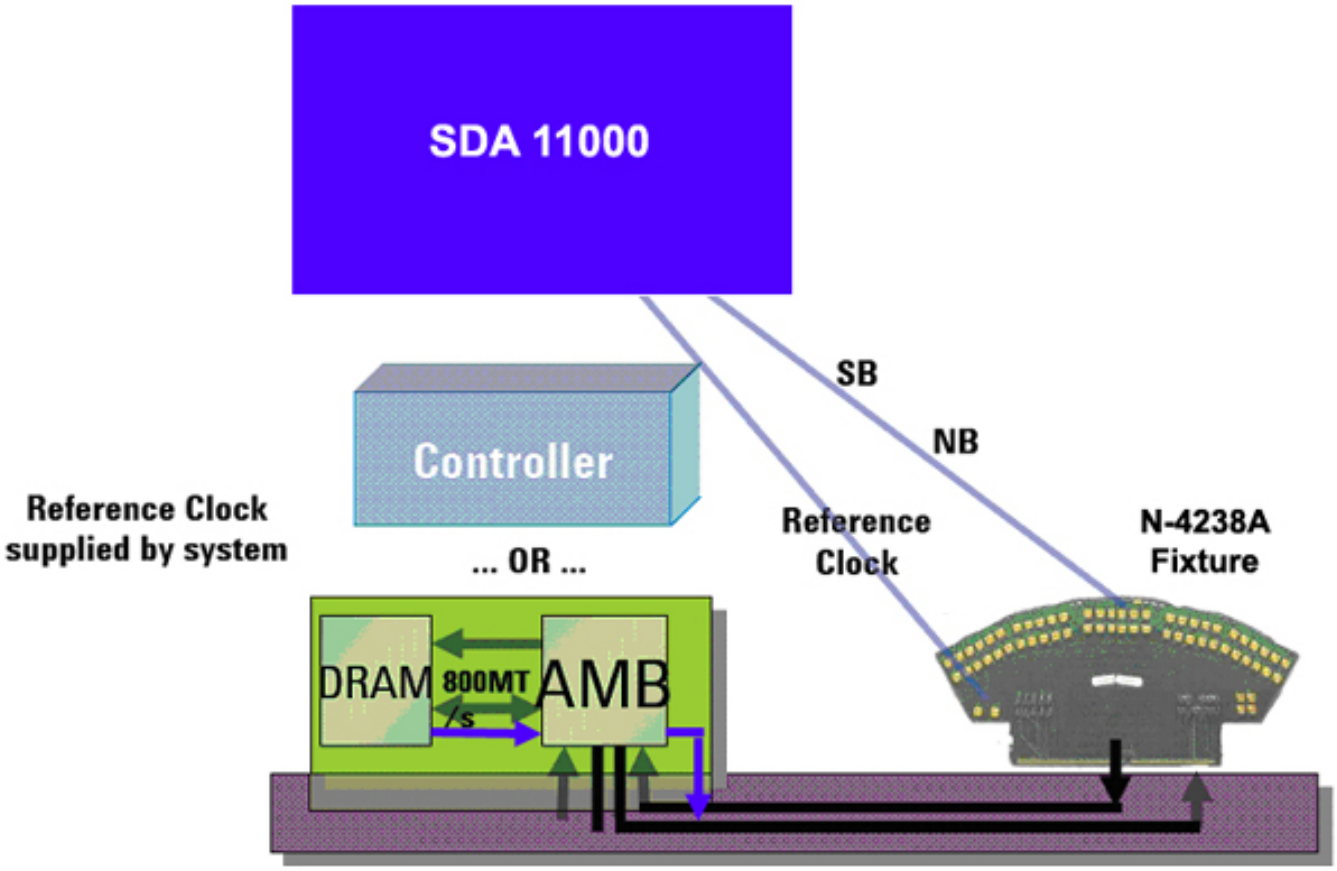
X-Replay allows you to export the entire test sessions to XML file for subsequent access by database programs such as Microsoft Access. Most database programs have built-in XML import data capability. Please note that test sessions appear at the lower left portion of X-Replay screen.

In order to create an XML record of the session data, select **Create XML** in the Reports Generator dialog:



Saving test results to *xml format

REFERENCE CLOCK TESTS



1.1 Reference Clock Frequency

Purpose of Measurement: Measure the nominal frequency of differential reference clock, not including Jitter and Spread spectrum.

Fixtures Required

- differential probe (D600 or D11000) connected directly to the FB-DIMM module.
- CTC or certified Motherboard
- N4238A fixture inserted into a slot of the main board or CTC

Test Procedure

1. Connect probe(s) to measure reference clock. Probe the differential clock directly on the FB-DIMM module, using a differential probe D600 connected to CH1
2. Insert N4238A into a slot. Connect calibrated SMA-to-SMP cables from "Reference Clock Output" to CH1 and CH2.
3. Follow the prompts in X-Replay as required.

Measurement Algorithm

1 / (mean value of clock period over all periods in acquisition window)

Reference

Symbol	Parameter	Min	Max	Units	Notes
$f_{Refclk-3.2}$	Reference clock frequency @ 3.2 Gb/s (nominal 133.33 MHz)	126.67	133.40	MHz	1,2,3
$f_{Refclk-4.0}$	Reference clock frequency @ 4 Gb/s (nominal 166.67 MHz)	158.33	166.75	MHz	1,2,3
$f_{Refclk-4.8}$	Reference clock frequency @ 4.8 Gb/s (nominal 200 MHz)	190.00	200.10	MHz	1,2,3

Notes:

1. The nominal reference clock frequency is determined by the data frequency of the link divided by 2 times the fixed PLL multiplication factor for the FB-DIMM channel (6:1). f_{data} = 2000 MHz for a 4.0 Gb/s FB-DIMM channel and so on.

2. Measured with SSC disabled. Enabling SSC will reduce the reference clock frequency as described in section 3.1.2.

3. Not all FB-DIMM agents will support all frequencies; compliance to the frequency specifications is only required for those data rates that are supported by the device under test.

1.2, 1.3: Single Ended Maximum and Minimum Clock Voltages

Purpose of Measurement: Measure the absolute ranges of single-ended signals.

Fixtures Required

- differential probe (D600) connected directly to the FB-DIMM module.
- CTC or certified Motherboard
- N4238A fixture inserted into a slot of the main board or CTC

Test Procedure

1. Insert N4238A into a slot.
2. Connect calibrated SMA cables from "Reference Clock Output" to CH1 and CH2. Set up a mathematical function as CH1 - CH2, this is the differential input.
3. Measure all the Maximum and Minimum values of each single lines and check against limits.

Measurement Algorithm

Maximum(CH1), Maximum(CH2), Minimum(CH1), Minimum(CH2)

Reference

Symbol	Parameter	Min	Max	Units	Notes
V_{max}	Single-ended maximum voltage		1.15	V	4,6
V_{min}	Single-ended minimum voltage	-0.3		V	4,7

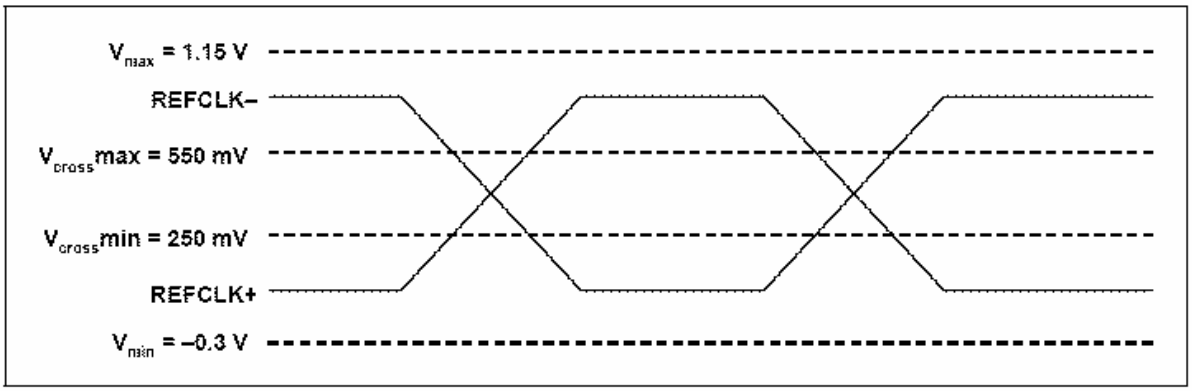
Notes:

4. Measurement taken from **single-ended waveform**.

6. Defined as the maximum instantaneous voltage including overshoot. See Figure 3-3.

7. Defined as the minimum instantaneous voltage including undershoot See Figure 3-3.

Figure 3-3. Single-ended Maximum and Minimum Levels and V_{cross} Levels



Reference

Symbol	Parameter	Min	Max	Units	Notes
V_{cross}	Absolute crossing point	250	550	mV	4,8,9

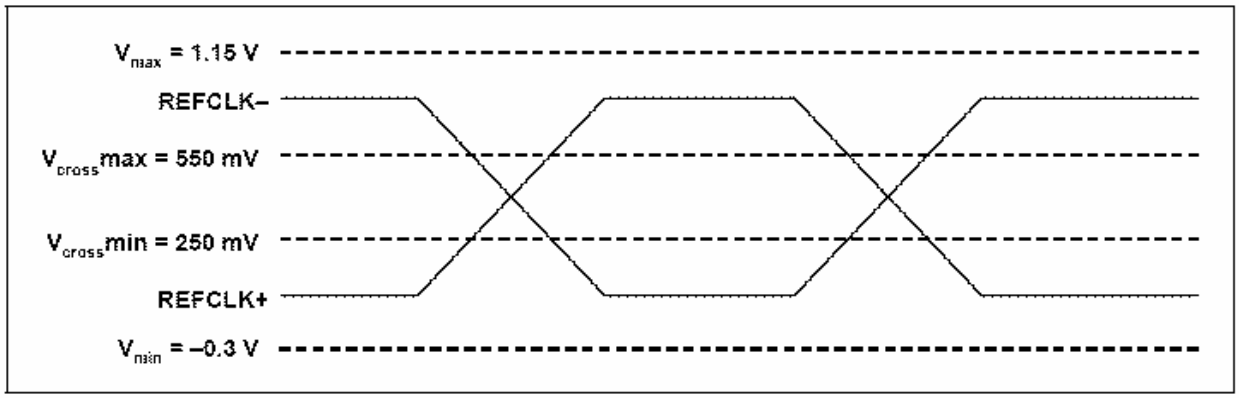
Notes:

4. Measurement taken from **single-ended waveform**.

8. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 3-3.

9. Refers to the total variation from the lowest crossing pint to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 3-3.

Figure 3-3. Single-ended Maximum and Minimum Levels and V_{cross} Levels



Measurement Algorithm

Vcross(C1,C2).min and Vcross(C1,C2).max -> Note : Vcross() set to 'Both' to measure all cross (as note 9 says).

1.4 Absolute Crossing Point

Purpose of Measurements: Measure the peak-to-peak variation of absolute voltage where the rising edge of REFCLK+ crosses the falling edge of REFCLK-.

Fixtures Required

- differential probe (D600) connected directly to the FB-DIMM module.
- CTC or certified Motherboard

- N4238A fixture inserted into a slot of the main board or CTC

Test Procedure

1. Insert N4238A into a slot. Connect calibrated SMA-to-SMP cables from "Reference Clock Output" to CH1 and CH2.
2. Measure all these cross levels, where REFCLK+ cross REFCLK-.

Measurement Algorithm

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{cross\text{-}delta}$	V_{cross} variation		140	mV	4,8,10

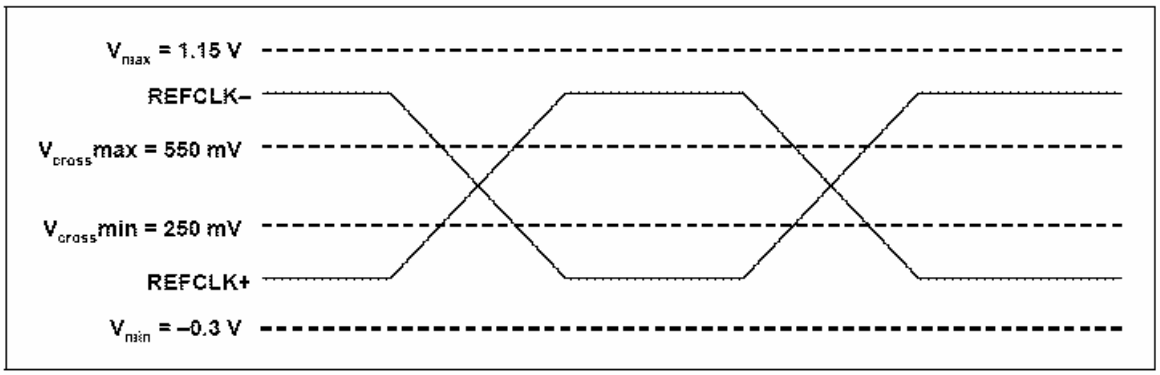
Notes:

4. Measurement taken from **single-ended waveform**.

8. Measured at the crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 3-3.

10.Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in for any particular system. See Figure 3-4.

Figure 3-3. Single-ended Maximum and Minimum Levels and V_{cross} Levels



Fixture: N4238A fixture inserted into a slot of the main board

Test Procedure

1. Insert N4238A into a slot. Connect calibrated SMA cables from "Reference Clock Output" to CH1 and CH2. Setup a mathematical function as CH1 - CH2, this is the differential input.
2. Set up vertical gain and offset to correctly fill the ADC range.
3. Set up the acquisition window to 400 µs, 10 GS/s.
4. Measure all these cross levels (see note 8, only on REFCLK+ rising edges, not falling edges).
5. Calculate Min - Max and check that it's smaller than the reference limit.

Measurement Algorithm

Vcross(C1,C2).min and Vcross(C1,C2) max.

1.5 Voltage Crossing Variation

Purpose: Measure the slew rate within the Vil and Vih transition levels

Fixtures Required

- differential probe (D600) connected directly to the FB-DIMM module.
- CTC or certified Motherboard
- N4238A fixture inserted into a slot of the main board or CTC

Test Procedure

1. Connect probe(s) to measure reference clock. Probe the differential clock directly on the FB-DIMM module, using a differential probe D600 connected to CH1
2. Insert N4238A into a slot. Connect calibrated SMA cables from "Reference Clock Output" to CH1 and CH2. Measure Average against limit.

Reference

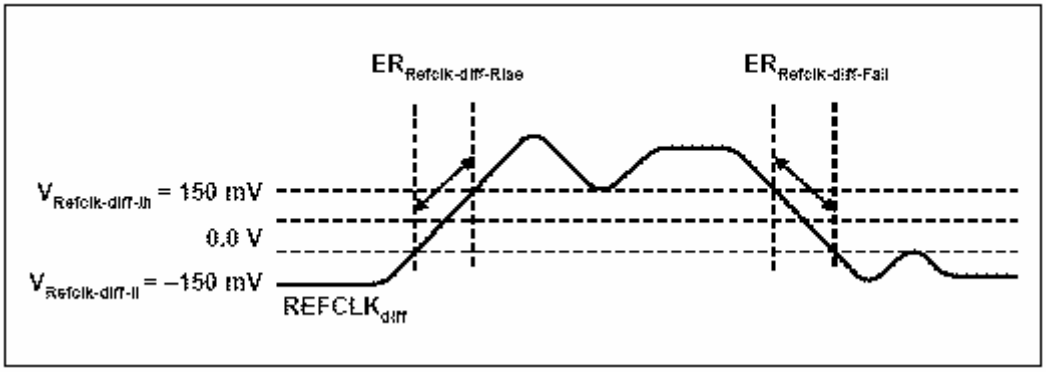
Symbol	Parameter	Min	Max	Units	Notes
$ER_{Refclk\text{-}diffRise}$ $ER_{Refclk\text{-}diffFall}$	Rising and falling edge rates	0.6	4.0	V/ns	5,12

Notes:

5. Measurement taken from **differential waveform**.

12.Measured from -150 mV to + 150 mV on the differential waveform. The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential 0 V crossing. See Figure **3-5** below:

Figure 3-5. Differential Edge Rate Definition



Measurement Algorithm:

Vcross(C1,C2).max - Vcross(C1,C2).min

1.6, 1.7 and 1.8: Rising and Falling Edge Rate Variation and Mismatch

Purpose of Measurement: Measure mismatch between rise and fall times of single-ended lines.

Fixtures Required

- differential probe (D600) connected directly to the FB-DIMM module.
- CTC or certified Motherboard
- N4238A fixture inserted into a slot of the main board or CTC

Test Procedure

1. Insert N4238A into a slot. Connect calibrated SMA-to-SMP cables from "Reference Clock Output" to CH1 and CH2. 2
2. Follow the X-Replay prompts as needed.

Reference

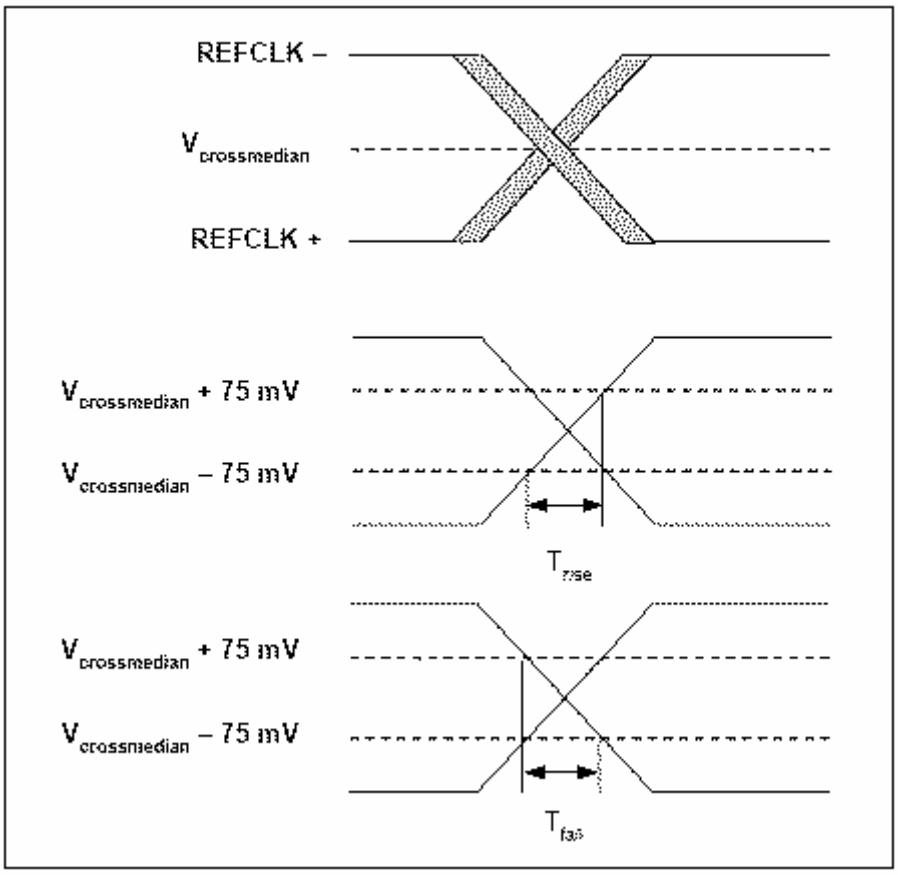
Symbol	Parameter	Min	Max	Units	Notes
$ER_{Refclk-Match}$	% mismatch between rise and fall edge rates		20	%	4,13

Notes:

4. Measurement taken from **single-ended waveform**.

13.Edge rate matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The **median cross point** is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations. The rising edge rate of REFCLK+ should be compared to the falling edge rate of REFCLK-. The maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure **3-6**.

Figure 3-6. Rise and Fall Time Definition (for $ER_{Refclk-Match}$ only)



Measurement Algorithms

Rising and Falling Edge Rate: **Slew(F1).mean**

% Rising/Falling Edge Mismatch**:**

1.9 Duty Cycle of Reference Clock

Purpose of Measurement: Measure the duty cycle on the REFCLK waveform.

Fixtures Required

- differential probe (D600) connected directly to the FB-DIMM module.

- CTC or certified Motherboard
- N4238A fixture inserted into a slot of the main board or CTC

Test Procedure

1. Connect probe(s) to measure reference clock. Probe the differential clock directly on the FB-DIMM module, using a differential probe D600 connected to CH1.
2. Insert N4238A into a slot. Connect calibrated SMA-to-SMP cables from "Reference Clock Output" to CH1 and CH2. Measure the Average duty cycle at 0V differential level

Reference

Symbol	Parameter	Min	Max	Units	Notes
$T_{Refclk\text{-}Dutycycle}$	Duty cycle of reference clock	40	60	%	5

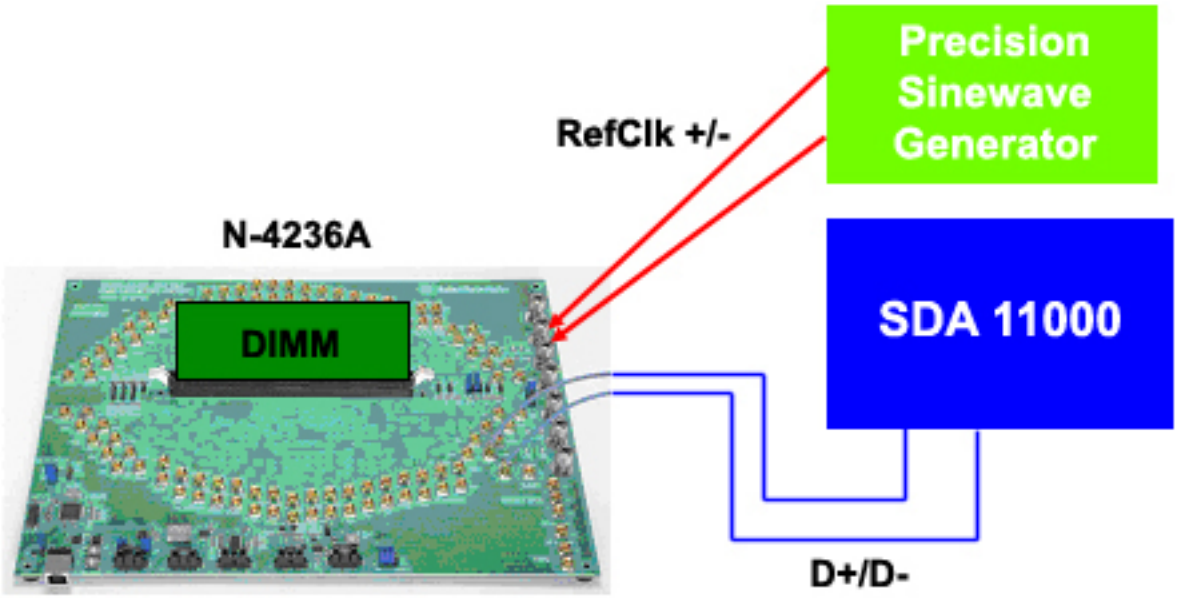
Notes:

5. Measurement taken from differential waveform.

Measurement Algorithm

The mean value of **Duty@lvl at 0 V** for the differential signal

TRANSMITTER TESTS



2.1, 2.2, 2.3 Differential Peak-to-Peak Output Voltage for Small Regular and Large Voltage Swing

Purpose of Measurement: Measure the minimum and maximum differential voltage swing for No-de-emphasis bits.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Connect probe(s) to measure reference clock. Probe the TX output directly on the FB-DIMM module, using a differential probe D11000 connected to CH1
2. Insert FB-DIMM module into N4236A . Connect calibrated SMA cables from "TX Output" to CH1 and CH2.
3. Set up the source to provide 101010 pattern. See specific instructions for setting up IBIST in N4236A software instructions.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{TX-DIFFp-p\_L}$	Differential peak-to-peak output voltage for large voltage swing	900	1300	mV	$V_{TX-DIFFp-p}$ = 2 * | V_{TX-D+} - V_{TX-D-} | Measured as Note 1
$V_{TX-DIFFp-p\_R}$	Differential peak-to-peak output voltage for regular voltage swing	800			$V_{TX-DIFFp-p}$ = 2 * | V_{TX-D+} - V_{TX-D-} | Measured as Note 1
$V_{TX-DIFFp-p\_S}$	Differential peak-to-peak output voltage for small voltage swing	520			$V_{TX-DIFFp-p}$ = 2 * | V_{TX-D+} - V_{TX-D-} | Measured as Note 1

Notes:

1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a **101010 pattern**.

Measurement Algorithm

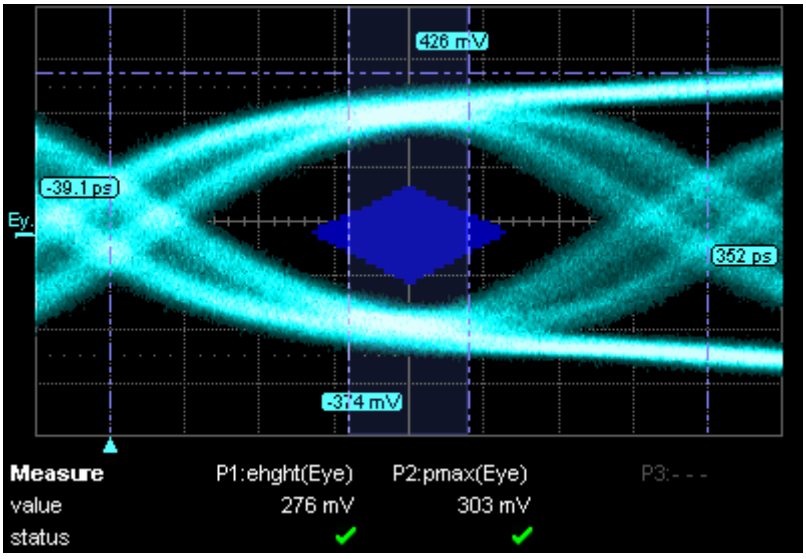
Note : EyeHeight is a measurement made from the histogram of persistence slice from eye aperture. Eye aperture for NRZ is 0.2 UI at the center of the eye. Eye height is measured with this formula :

```
EyeHeight = (OneLevel - 3*SigmaOne) - (ZeroLevel + 3*SigmaZero)
```

Scope Setup

Eye Height(Eye) > Min

Persist Max(Eye) < Max measurement made on 1 UI.



2.4, 2.5: DC Common Mode Output Voltage for Small and Large Voltage Swing

Purpose of Measurement: Measure the DC Common mode voltage of transmitter output.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR

- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Insert FB-DIMM module into N4236A . Connect calibrated SMA cables from "TX Output" to CH1 and CH2.
2. Set up the source to provide 101010 pattern. See specific instructions for setting up IBIST in N4236A software instructions.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{TX-CM-L}$	DC common code output voltage for large voltage swing		375	mV	Defined as: V_{TX-CM} = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ Measured as: Note 1
V_{TX-CM_S}	DC common mode output voltage for small voltage swing	135	280	mV	Defined as: V_{TX-CM} = $DC_{(avg)}$ of $\|V_{TX-D+} + V_{TX-D-}\|/2$ Measured as: Note 1 See also Note 2

Notes:

1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a **101010 pattern.**

2. The transmitter designer should not artificially elevate the common mode in order to meet this specification.

Measurement Algorithm:

Mean(LowPass((C1 + C2) / 2))) -> filter : low pass at 30 kHz

2.6: De-emphasized Differential Output Voltage Ratio for -3.5 and -6 dB

Purpose of Measurement : Measure the de-emphasized level

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Connect probe(s) to measure reference clock. Probe the TX output directly on the FB-DIMM module, using a D11000 differential probe connected to CH1
2. Insert FB-DIMM module into N4236A . Connect calibrated SMA-to-SMP cables from "TX Output" to CH1 and CH2.
3. Set up the source to provide 1 x UserPattern[0x0f3355] (see section 4.5)

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{TX\text{-}DE\text{-}3.5\text{-}Ratio}$	De-emphasized differential output voltage ratio for -3.5 dB de-emphasis	-3.0	-4.0	dB	1,3,4
$V_{TX\text{-}DE\text{-}6.0\text{-}Ratio}$	De-emphasized differential output voltage ratio for -6.0 dB de-emphasis	-5.0	-7.0	dB	1,3,4

Notes:

1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a 101010 pattern.

3. This is the ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition.

4. De-emphasis shall be disabled in the calibration state.

Measurement Algorithm

Using VTxDE(F1) as for PCIe

```
//    Algorithm:
//    1. Walk the waveform.
//    2. Detect a transition in the NRZ signal using time@level. Call it
t0.
//    3. Measure the voltage at t0+0.5period and t0+1.5Period and add it
to a running average
//    4. The voltage at t0+0.5period is the voltage of the emphesized bit
//    5. The voltage at t0+1.5period might be the voltage of the de-
emphesized bit but might
//       be the voltage of another emphesized bit. Run this voltage
through a decision maker
//    6. Output a value that is Vde/Vem in units of db.
```

2.7, 2.8, 2.9: AC Peak-to-Peak Common Mode Output Voltage Ratio for Small, Regular and Large Voltage Swings

Purpose of Measurements: Measure the peak-to-peak AC component of common mode voltage.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Insert FB-DIMM module into N4236A . Connect calibrated SMA-to-SMP cables from "TX Output" to CH1 and CH2.
2. Set up the source to provide 101010 pattern

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{TX\text{-}CM\text{-}ACp\text{-}p\ L}$	AC peak-to-peak common mode output voltage for large swing		90	mV	$V_{TX\text{-}CM\text{-}AC}$ = Max $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ - Min $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ Measured as: Note 1 See also Note 5
$V_{TX\text{-}CM\text{-}ACp\text{-}p\ R}$	AC peak-to-peak common mode output voltage for regular swing		80	mV	$V_{TX\text{-}CM\text{-}AC}$ = Max $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ - Min $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ Measured as: Note 1 See also Note 5
$V_{TX\text{-}CM\text{-}ACp\text{-}p\ S}$	AC peak-to-peak common mode output voltage for small swing		70	mV	$V_{TX\text{-}CM\text{-}AC}$ = Max $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ - Min $\lvert V_{TX\text{-}D+} + V_{TX\text{-}D-}\rvert/2$ Measured as: Note 1 See also Note 5

Notes:

1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a 101010 pattern.

5. Includes all sources of AC common mode noise.

Spec 1.3.5 says AC is above 30 kHz

Measurement Algorithm

Pkpk(high pass filter((C1 + C2) / 2))) filter: high-pass at 30 kHz

2.10: Maximum Single-ended Voltage in EI (Electrical Idle) Condition, DC+AC

Purpose of Measurement: Measure the maximum single-ended voltage in Electrical Idle condition.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Insert FB-DIMM module into N4236A fixture. Connect calibrated SMA-to-SMP cables from "TX Output" to CH1 and CH2. Set up a mathematical function as CH1 - CH2; this is the differential input.
2. Set up the source to **Electrical Idle mode**. See N4236A fixture documentation for details

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{TX\text{-}IDLE\text{-}SE}$	Maximum single-ended voltage in EI condition, DC + AC		50	mV	6,7

Notes:

6. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition.

7. Specified at the package pins into a voltage compliance test load. Transmitters must meet both single-ended and differential output EI specifications.

Measurement Algorithm

Maximum(C1), Maximum(C2)

2.11: Maximum Single-ended Voltage in EI (Electrical Idle) Condition, DC Only (2.11)

Purpose of Measurement: Measure the DC-only maximum single-ended voltage in Electrical Idle condition.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMP-to-SMA cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Insert FB-DIMM module into N4236A . Connect calibrated SMA-to-SMP single-ended cables from "TX Output" to CH1 and CH2.
2. Set up the source to **Electrical Idle mode**.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{TX-IDLE-SE-DC}$	Maximum single-ended voltage in EI condition, DC only		20	mV	6,7,8

Notes:

6. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition.

7. Specified at the package pins into a voltage compliance test load. Transmitters must meet both single-ended and differential output EI specifications.

8. This specification, considered with $V_{RX-IDLE-SE-DC}$, implies a maximum 15 mV single-ended DC offset between TX and RX pins during the electrical idle condition. This in turn allows a ground offset between adjacent FB-DIMM agents of 26 mV when worst-case termination resistance matching is considered.

Measurement Algorithm

Maximum(FFTFilter(C1)), Maximum(FFTFilter(C2))

2.12: Maximum Peak-to-Peak Differential Voltage in EI Condition

Purpose of Measurement: Measure the maximum peak-to-peak differential voltage in Electrical Idle condition.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Connect probes to measure reference clock. Probe the TX output directly on the FB-DIMM module, using a differential probe D11000 connected to CH1.
2. Insert FB-DIMM module into N4236A . Connect calibrated SMA-to-SMP cables from "TX Output" to CH1 and CH2.
3. Set up the source to **Electrical Idle mode**.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{TX\text{-}IDLE\text{-}DIFFp\text{-}p}$	Maximum peak-to-peak differential voltage in EI condition		40	mV	7

Notes:

7. Specified at the package pins into a voltage compliance test load. Transmitters must meet both single-ended and differential output EI specifications.

Measurement Algorithm:

Peak to Peak(C1-C2)

2.13: Single ended Voltage in D+/D-

Purpose of Measurement : Measure the minimum and maximum voltage on single-ended lines.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Insert FB-DIMM module into N4236A . Connect calibrated SMA-to-SMP cables from "TX Output" to CH1 and CH2.
2. Set up the source to provide **101010 pattern**

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{TX\text{-}SE}$	Single -ended voltage (w.r.t. VSS) on D+/D-	-75	750	mV	1,9

Notes:

1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a **101010 pattern.**

9. The maximum value is specified to be at least ($V_{TX\text{-}DIFFp\text{-}p\ L}$ / 4) + $V_{TX\text{-}CM\ L}$ + ($V_{TX\text{-}CM\text{-}ACp\text{-}p}$ / 2)

Measurement Algorithm

Minimum(C1), Minimum(C2) > Minimum

Maximum(C1), Maximum(C2) < Maximum

2.14: Minimum Tx Eye Width

Purpose of Measurement: Measure the minimum eye width.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMP-to-SMA cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Connect probe(s) to measure reference clock. Probe the TX output directly on the FB-DIMM module, using a differential probe D11000 connected to CH1.
2. Insert FB-DIMM module into N4236A . Connect calibrated SMA-to-SMP cables from "TX Output" to CH1 and CH2.
3. Set up the source to provide 101010 pattern.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$T_{TX-Eye-MIN}$	Minimum TX eye width, 3.2 and 4.0 Gb/s	0.7		UI	1,10
$T_{TX-Eye-MIN-4.8}$	Minimum TX eye width, 4.8 Gb/s	TBD		UI	1,10

Notes:

1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a **101010 pattern.**

10.This number does not include the effects of SSC or reference clock jitter.

Measurement Algorithm

Note: Eye Width is calculated with this formula from a histogram of data sliced horizontally at cross level :

(TCross2 - JittertRMS2) - (TCross1 + JitterRMS1)

EyeWidth (Eye)

2.15 Maximum Tx Deterministic Jitter(2.15)

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

TO BE DEFINED

Reference

Symbol	Parameter	Min	Max	Units	Notes
$T_{TX-DJ-DD}$	Maximum TX deterministic jitter, 3.2 and 4.0 Gb/s		0.2	UI	1,10,11
$T_{TX-DJ-DD-4.8}$	Maximum TX deterministic jitter, 4.8 Gb/s		TBD	UI	1,10,11

Notes:

1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a **101010 pattern.**

10.This number does not include the effects of SSC or reference clock jitter.

11.Defined as the dual-dirac deterministic jitter as described in Section 4.

2.16: Instantaneous Pulse Width

Purpose of Measurement : Measure the minimum pulse width with a 0 V differential level.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1) Connect probe(s) to measure reference clock. Probe the TX output directly on the FB-DIMM module, using a differential probe D11000 connected to CH1
2) Insert FB-DIMM module into N4236A . Connect calibrated SMA cables from "TX Output" to CH1 and CH2.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$T_{TX-PULSE}$	Instantaneous pulse width	0.85		UI	12

Notes:

12. Pulse width measured at 0 V differential.

Measurement Algorithm

Width@0Volt (F1).Min F1 is C1-C2

2.17, 2.18: Differential Tx Output Rise / Fall Time

Purpose of Measurement: Measure the rise and fall times of Tx differential lines.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Connect probe(s) to measure reference clock. Probe the TX output directly on the FB-DIMM module, using a differential probe D11000 connected to CH1
2. Insert FB-DIMM module into N4236A . Connect calibrated SMA cables from "TX Output" to CH1 and CH2.
3. Set up the source to provide 101010 pattern

Reference

Symbol	Parameter	Min	Max	Units	Notes
$T_{TX\text{-}RISE}$ $T_{TX\text{-}RISE}$	Differential TX output rise/fall time	30	90	ps	Given by 20% -80% voltage levels. Measured as: Note 1

Notes:

1. Specified at the package pins into a timing and voltage compliance test load. Common-mode measurements to be performed using a 101010 pattern.

Fixtures

- differential probe (D11000PS) connected directly to the FB-DIMM module.
- FB-DIMM module inserted in a N4236A fixture.

Measurement Algorithm

Rise2080(F1).mean

Fall8020(F1).mean F1 is C1-C2

2.19: Mismatch between Rise / Fall Times

Purpose of Measurement : Measure the difference between rise and fall times of differential signal.

Fixtures

- Differential probe (D11000PS) connected directly to the FB-DIMM module, OR
- SMA-to-SMP cables for D+ and D- single-ended measurements
- FB-DIMM module (DUT) inserted in a N4236A fixture.
- Reference Clock Source (Precision Sinewave Generator) running at 133, 166, or 200 MHz

Test Procedure

1. Connect probe(s) to measure reference clock. Probe the TX output directly on the FB-DIMM module, using a differential probe D11000 connected to CH1
2. Insert FB-DIMM module into N4236A . Connect calibrated SMA cables from "TX Output" to CH1 and CH2.
3. Set up the source to provide 101010 pattern

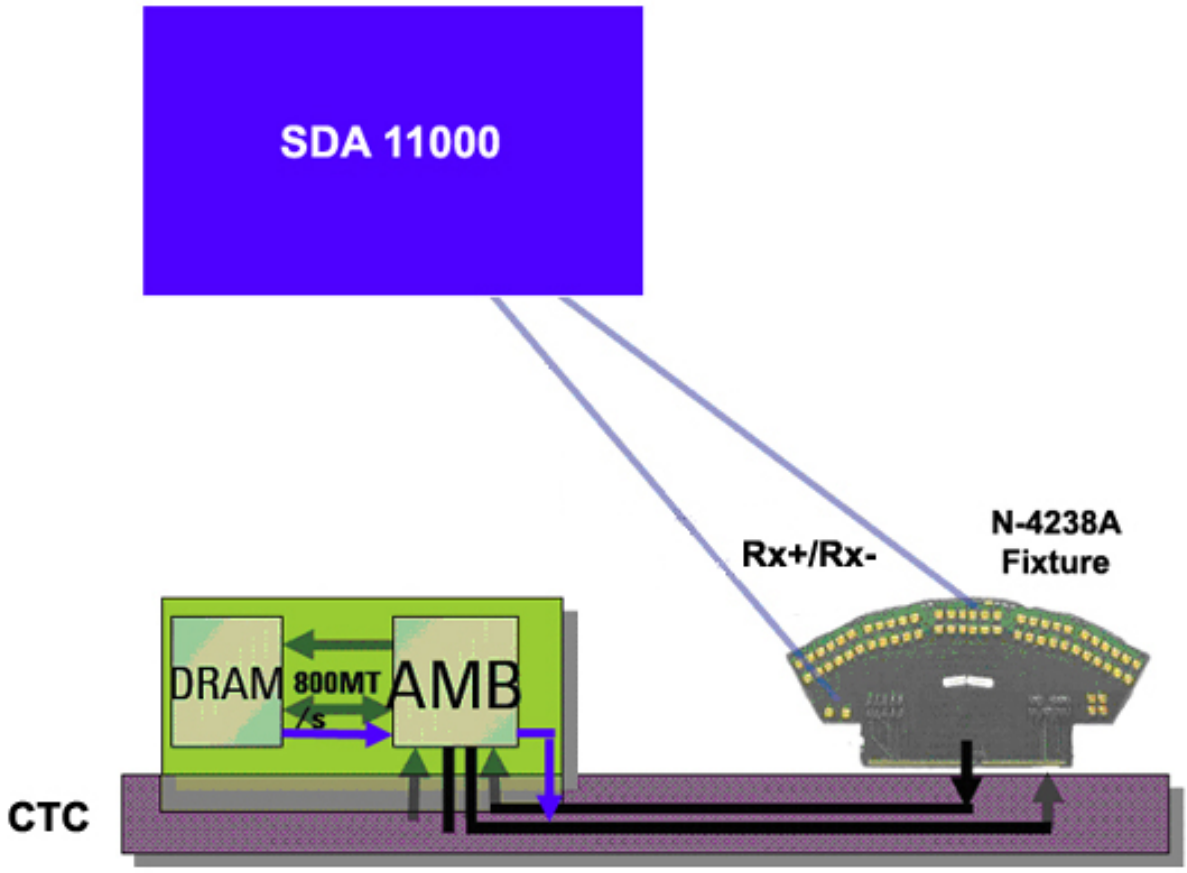
Reference

Symbol	Parameter	Min	Max	Units	Notes
$T_{TX\text{-}RF\text{-}MISMATCH}$	Mismatch between rise and fall times		20	ps	

Measurement Algorithm

abs(Rise2080(F1) - Fall8020(F1)) < Max, F1 is C1-C2

RECEIVER TESTS



3.1: Differential Peak to Peak input Voltage

Purpose of Measurement: Measure the minimum and maximum differential input voltage.

Fixtures Required

- Differential probe (D11000PS) connected directly to the FB-DIMM module OR
- SMA-to-SMP single-ended cables.
- CTC or certified Motherboard.
- N4238A fixture inserted into a slot of the main board or CTC.

Test Procedure

1. Connect probe(s) to measure reference clock. Probe the TX output directly on the FB-DIMM module, using a differential probe D600 connected to CH1
2. Insert N4238A into a slot. Connect calibrated SMA cables from "TX Output" to CH1 and CH2.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{RX\text{-}DIFFp\text{-}p}$	Differential peak-to-peak input voltage	170	1300	mV	$V_{RX\text{-}DIFFp\text{-}p} = 2*\lvert V_{RX\text{-}D+} - V_{RX\text{-}D\text{-}}\rvert$ Measured as: Note 1

Notes:

1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.

Measurement Algorithm

Eye Height(Eye) > Min

Persist Max(Eye) < Max

3.2: Maximum Single ended Voltage for EI Condition, DC+AC

Purpose of Measurement : Measure the maximum single-ended voltage in Electrical Idle condition.

Fixtures Required

- Differential probe (D11000PS) connected directly to the FB-DIMM module OR
- SMA-to-SMP single-ended cables.
- CTC or certified Motherboard.
- N4238A fixture inserted into a slot of the main board or CTC.

Test Procedure

1. Insert N4238A into a slot. Connect calibrated SMA cables from "TX Output" to CH1 and CH2.
2. Set up the source to **Electrical Idle mode**.
3. Measure the Maximum voltage on each single-ended line.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{RX-IDLE-SE}$	Maximum single-ended voltage for EI condition (AC + DC)		75	mV	2,3,4,5

Notes:

2. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition. Worst-case margins are determined by comparing EI levels with common mode levels during normal operation for the case with transmitter using small voltage swing. See Figure 3-16 and Figure 3-17.

3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.

4. Specified at the package pins into a timing and voltage compliance test setup.

5. Receiver designers may implement either single-ended or differential EI detection. Receivers must meet the specification that corresponds to the implemented detection circuit.

Figure 3-16. RX Single-ended Electrical Idle Levels

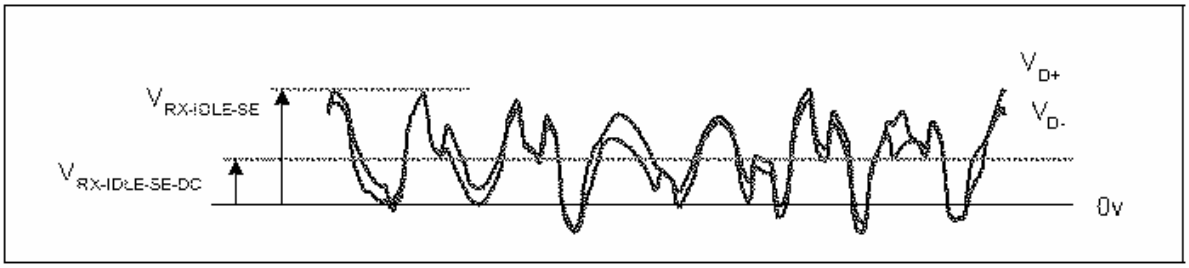
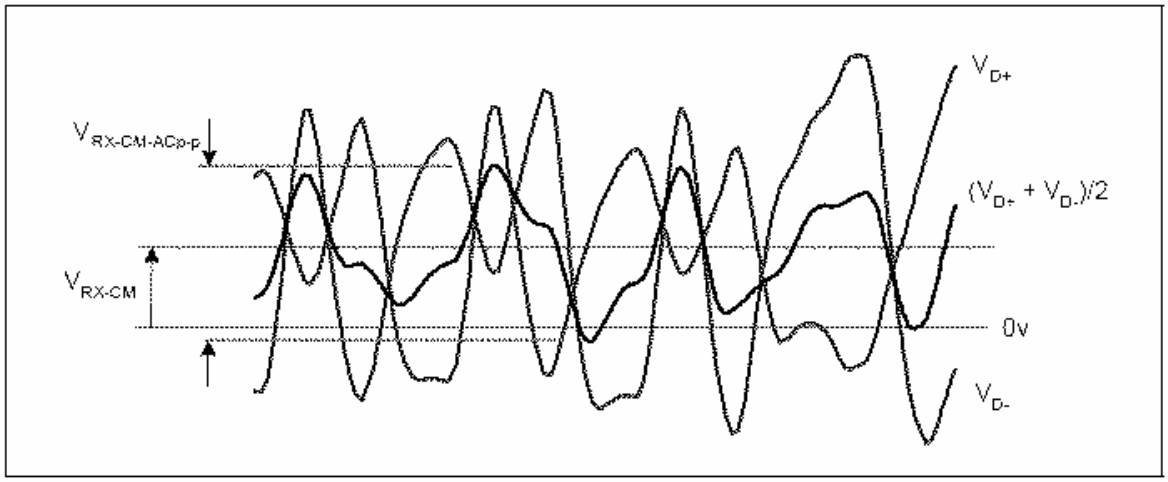


Figure 3-17. RX Common Mode Levels during Normal Operation (Small Swing Setting)



Measurement Algorithm

Maximum(C1), Maximum(C2)

3.3: Maximum Peak-to-Peak Differential Voltage for EI Condition

Purpose of Measurement: Measure the maximum peak-to-peak differential voltage in Electrical Idle condition.

Fixtures Required

- Differential probe (D11000PS) connected directly to the FB-DIMM module OR
- SMA-SMP single-ended cables.
- CTC or certified Motherboard.
- N4238A fixture inserted into a slot of the main board or CTC.

Test Procedure

1. Probe the RefClk input directly on the FB-DIMM module, using a differential probe D11000 connected to CH1.
2. Insert N4238A into a slot. Connect calibrated SMA-to-SMP cables from "RX Input" to CH1 and CH2.
3. Set up the source to **Electrical Idle mode**.
4. Measure the peak-to-peak voltage on differential signal.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{RX-IDLE-DIFFp-p}$	Maximum peak-to-peak differential voltage for EI condition		65	mV	3,4,5

Notes:

3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.

4. Specified at the package pins into a timing and voltage compliance test setup.

5. Receiver designers may implement either single-ended or differential EI detection. Receivers must meet the specification that corresponds to the implemented detection circuit.

Measurement Algorithm

Peak to Peak(C1-C2)

3.4: Single-ended Voltage on D+/ D-

Purpose of Measurement: Measure the minimum and maximum voltage on single-ended lines.

Fixtures Required

- Differential probe (D11000PS) connected directly to the FB-DIMM module OR
- SMA-SMP single-ended cables.
- CTC or certified Motherboard.
- N4238A fixture inserted into a slot of the main board or CTC.

Test Procedure

1. Insert N4238A into a slot. Connect calibrated SMA cables from "TX Output" to CH1 and CH2.
2. Measure the Minimum and Maximum voltage and check against limits.

Reference

Symbol	Parameter	Min	Max	Units	Notes
V_{RX-SE}	Single -ended voltage (w.r.t. VSS) on D+/D-	-300	900	mV	4

Notes:

4. Specified at the package pins into a timing and voltage compliance test setup.

Measurement Algorithm

Minimum(C1), Minimum(C2) > Minimum

Maximum(C1), Maximum(C2) < Maximum

3.5: Maximum Rx Inherent Deterministic Timing Error

Purpose : TBD

Fixtures Required

- Differential probe (D11000PS) connected directly to the FB-DIMM module OR
- SMA-to-SMP single-ended cables.
- CTC or certified Motherboard.
- N4238A fixture inserted into a slot of the main board or CTC.

Test Procedure

1. Probe the TX output directly on the FB-DIMM module, using a differential probe D600 connected to CH1
2. Insert N4238A into a slot. Connect calibrated SMA cables from "TX Output" to CH1 and CH2. Set up a mathematical function as CH1 - CH2, this is the differential input.
3. Set up the source to provide 101010 pattern.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$T_{RX-DJ-DD}$	Maximum RX deterministic jitter, 3.2 and 4.0 Gb/s		0.3	UI	4,9,10,11
$T_{RX-DJ-DD-4.8}$	Maximum RX deterministic jitter, 4.8 Gb/s		TBD	UI	4,9,10,11

Notes:

4. Specified at the package pins into a timing and voltage compliance test setup.

9. This number does not include the effects of SSC or reference clock jitter.

10. This number includes setup and hold of the RX sampling flop.

11. Defined as the dual-dirac deterministic timing error as described in Section 4.

3.6: DC Common Mode of the Input Voltage

Purpose of Measurement : Measure the DC Common mode voltage of transmitter input.

Fixtures Required

- Differential probe (D11000PS) connected directly to the FB-DIMM module OR
- SMA-SMP single-ended cables.
- CTC or certified Motherboard.
- N4238A fixture inserted into a slot of the main board or CTC.

Test Procedure

1. Insert N4238A into a slot. Connect calibrated SMA-to-SMP cables from "TX Output" to CH1 and CH2.

Reference

Symbol	Parameter	Min	Max	Units	Notes
V_{RX-CM}	Common mode of the input voltage	120	400	mV	Defined as: $V_{RX-CM} = DC_{(avg)}$ of $\lvert V_{RX-D+} + V_{RX-D-}\rvert/2$ Measured as: Note 1 See also Note 12

Notes:

1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.

12. Allows for 15 mV DC offset between transmit and receive devices.

Measurement Algorithm

Mean(FFTFilter((C1 + C2) / 2))) -> filter : low pass at 30 kHz

3.7: AC Peak-to-Peak Common Mode of the Input Voltage

Purpose of Measurement : Measure the peak-to-peak AC component of common mode voltage.

Fixtures Required

- Differential probe (D11000PS) connected directly to the FB-DIMM module OR
- SMA-SMP single-ended cables.
- CTC or certified Motherboard.
- N4238A fixture inserted into a slot of the main board or CTC.

Test Procedure

1. Insert N4238A into a slot. Connect calibrated SMA-to-SMP cables from "TX Output" to CH1 and CH2.
2. Measure AC common mode.

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{RX-CM-ACp-p}$	AC peak-to-peak common mode of input voltage		270	mV	$V_{RX-CM-AC}$ = Max $\|V_{RX-D+} + V_{RX-D-}\|/2$– Min $\|V_{RX-D+} + V_{RX-D-}\|/2$ Measured as: Note 1

Notes:

1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.

Measurement Algorithm :

PkPk(FFTFilter((C1 + C2) / 2))) -> filter: low-pass at 30 kHz

3.8: Ratio of $V_{RX-CM-ACp-p}$ to Minimum $V_{RX-DIFFp-p}$ (3.8)

Purpose of Measurement: Measure the peak-to-peak AC component of common mode voltage.

Fixtures Required

- Differential probe (D11000PS) connected directly to the FB-DIMM module OR
- SMA-SMP single-ended cables.
- CTC or certified Motherboard.
- N4238A fixture inserted into a slot of the main board or CTC.

Test Procedure

1. Insert N4238A into a slot. Connect calibrated SMA-to-SMP cables from "TX Output" to CH1 and CH2.
2. Set up the source to provide 101010 pattern.
3. Calculate: 100 * ($V_{RX-CM-ACp-p}$ / min($V_{RX-DIFFp-p}$))

Reference

Symbol	Parameter	Min	Max	Units	Notes
$V_{RX-CM-EH-Ratio}$	Ratio of $V_{RX-CM-ACp-p}$ to minimum $V_{RX-DIFFp-p}$		45	%	13

Notes:

13. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if $V_{RX-DIFFp-p}$ is 200 mV, the maximum AC peak-to-peak common mode is the lesser of (200 mV * 0.45 = 90 mV) and $V_{RX-CM-ACp-p}$.

Measurement Algorithm

100 * (Pkpk(FFTFilter((C1 + C2) / 2))) / Eye Height(Eye)) -> filter : high pass at 30 kHz

APPENDIX A – SAMPLE TEST REPORT

The following report displays all the parameters collected in the script. Availability of test parameter results depends on the chosen tests.

FB-DIMM PHY TESTS REPORT

Summary Table

Pass	Test	Measurement	Current Value	Test Criteria
●	1.2	VRefClk-max_p	799 mV	<= 1.150 V
●	1.2	VRefClk-max_n	821 mV	<= 1.150 V
●	1.3	VRefClk-min_p	-14 mV	>= -300 mV
●	1.3	VRefClk-min_n	-40 mV	>= -300 mV
●	1.4	VRefClk-cross-min	324.4 mV	>= 250.0 mV
●	1.4	VRefClk-cross-max	371.5 mV	<= 550.0 mV
●	1.5	VRefClk-cross-delta	3.97009047739004E-02	<=
●	1.8	ERRefClk-match	10.2999399960082	<=
●	1.1	fRefClk	200.056288 MHZ	190.00e6 < n < 200.10e6
●	1.6	TRefClk-rise	3.3187 GV/S	0.6e9 < n < 4.0e9
●	1.7	TRefClk-fall	3.0811 GV/S	0.6e9 < n < 4.0e9
●	1.9	TRefClk-dutycycle	49.29807 PCT	40 < n < 60
✕	1.10	TRefClk-jitter-rms	3.84 ps	<= 2.50 ps
●	2.4	VTX-CM_L	325 mV	<= 375 mV
●	2.7	VTX-CM-ACp-p_L	72.43 mV	<= 90.00 mV
●	2.13	VTX-SE-min_p	55 mV	-75e-3 < n < 750e-3
●	2.13	VTX-SE-min_n	63 mV	-75e-3 < n < 750e-3
●	2.13	VTX-SE-max_p	522 mV	-75e-3 < n < 750e-3
●	2.13	VTX-SE-max_n	519 mV	-75e-3 < n < 750e-3
●	2.8	VTX-CM-ACp-p_R	70.22 mV	<= 80.00 mV
●	2.5	VTX-CM_S	191 mV	135e-3 < n < 280e-3
●	2.9	VTX-CM-ACp-p_S	60.27 mV	<= 70.00 mV
●	2.10	VTX-IDLE-SE_p	7.7 mV	<= 50.0 mV
●	2.10	VTX-IDLE-SE_n	8.4 mV	<= 50.0 mV

Pass	Test	Measurement	Current Value	Test Criteria
●	2.11	VTX-IDLE-SE-DC_p	7.7 mV	<= 20.0 mV
●	2.11	VTX-IDLE-SE-DC_n	8.4 mV	<= 20.0 mV
✕	2.1	VTX-DIFFp-p_L-min	719 mV	>= 900 mV
●	2.1	VTX-DIFFp-p_L-max	886 mV	<= 1.300 V
✕	2.2	VTX-DIFFp-p_R-min	637 mV	>= 800 mV
✕	2.3	VTX-DIFFp-p_S-min	443 mV	>= 520 mV
●	2.14	TTX-eye-min	0.908850927739682	>=
●	2.17	TTX-rise	74.428 ps	30e-12 < n < 90e-12
●	2.18	TTX-fall	74.664 ps	30e-12 < n < 90e-12
●	2.19	TTX-RF-mismatch	2.36552061137673E-13	<=
✕	2.6.1	VTX-DE-3.5-ratio	-4.71406087786773	-3 < n < -4
✕	2.6.2	VTX-DE-6-ratio	-4.7473631144758	-5 < n < -7
●	2.16	TTX-pulse	0.863380579790157	>=
●	2.15	TTX-Dj	0.111908040420286	<=
●	2.12	VTX-IDLE-DIFFp-p	10.236 mV	<= 40.000 mV
●	3.4	VRX-SE-min_p	1 mV	-300e-3 < n < 900e-3
●	3.4	VRX-SE-min_n	-4 mV	-300e-3 < n < 900e-3
●	3.4	VRX-SE-max_p	324 mV	-300e-3 < n < 900e-3
●	3.4	VRX-SE-max_n	342 mV	-300e-3 < n < 900e-3
●	3.6	VRX-CM	196 mV	120e-3 < n < 400e-3
●	3.7	VRX-CM-ACp-p	71.81 mV	<= 270.00 mV
●	3.2	VRX-IDLE-SE_p	8.2 mV	<= 75.0 mV
●	3.2	VRX-IDLE-SE_n	8.9 mV	<= 75.0 mV
●	1.2	VRefClk-max_p	812 mV	<= 1.150 V
●	1.2	VRefClk-max_n	825 mV	<= 1.150 V
●	1.3	VRefClk-min_p	-20 mV	>= -300 mV
●	1.3	VRefClk-min_n	-40 mV	>= -300 mV
●	1.4	VRefClk-cross-min	325.8 mV	>= 250.0 mV
●	1.4	VRefClk-cross-max	370.8 mV	<= 550.0 mV

Pass	Test	Measurement	Current Value	Test Criteria
●	1.5	VRefClk-cross-delta	3.543405447868O5E-02	<=
●	1.8	ERRefClk-match	0.734923639691269	<=
●	1.1	fRefClk	133.032696 MHZ	190.00e6 < n < 200.10e6
●	1.6	TRefClk-rise	3.3029 GV/S	0.6e9 < n < 4.0e9
●	1.7	TRefClk-fall	3.0865 GV/S	0.6e9 < n < 4.0e9
●	1.9	TRefClk-dutycycle	49.56755 PCT	40 < n < 60
✕	1.10	TRefClk-jitter-rms	5.50 ps	<= 2.50 ps
✕	2.4	VTX-CM_L	494 mV	<= 375 mV
✕	2.7	VTX-CM-ACp-p_L	399.94 mV	<= 90.00 mV
●	2.13	VTX-SE-min_p	59 mV	-75e-3 < n < 750e-3
●	2.13	VTX-SE-min_n	43 mV	-75e-3 < n < 750e-3
●	2.13	VTX-SE-max_p	556 mV	-75e-3 < n < 750e-3
●	2.13	VTX-SE-max_n	581 mV	-75e-3 < n < 750e-3
✕	2.8	VTX-CM-ACp-p_R	357.90 mV	<= 80.00 mV
●	2.5	VTX-CM_S	276 mV	135e-3 < n < 280e-3
✕	2.9	VTX-CM-ACp-p_S	227.51 mV	<= 70.00 mV
●	2.10	VTX-IDLE-SE_p	6.4 mV	<= 50.0 mV
●	2.10	VTX-IDLE-SE_n	6.6 mV	<= 50.0 mV
●	2.11	VTX-IDLE-SE-DC_p	6.4 mV	<= 20.0 mV
●	2.11	VTX-IDLE-SE-DC_n	6.6 mV	<= 20.0 mV
✕	2.1	VTX-DIFFp-p_L-min	777 mV	>= 900 mV
●	2.1	VTX-DIFFp-p_L-max	1.000 V	<= 1.300 V
✕	2.2	VTX-DIFFp-p_R-min	629 mV	>= 800 mV
✕	2.3	VTX-DIFFp-p_S-min	430 mV	>= 520 mV
●	2.14	TTX-eye-min	0.866121578401112	>=
✕	2.17	TTX-rise	116.706 ps	30e-12 < n < 90e-12
✕	2.18	TTX-fall	133.471 ps	30e-12 < n < 90e-12
●	2.19	TTX-RF-mismatch	1.67649761846815E-11	<=
✕	2.6.1	VTX-DE-3.5-ratio	-4.82753882732286	-3 < n < -4

Pass	Test	Measurement	Current Value	Test Criteria
✗	2.6.2	VTX-DE-6-ratio	No Data Available	-5 < n < -7
●	2.16	TTX-pulse	0.858743838018372	>=
●	2.15	TTX-Dj	0.176261032196002	<=
●	2.12	VTX-IDLE-DIFFp-p	10.510 mV	<= 40.000 mV
●	3.4	VRX-SE-min_p	-8 mV	-300e-3 < n < 900e-3
●	3.4	VRX-SE-min_n	-14 mV	-300e-3 < n < 900e-3
●	3.4	VRX-SE-max_p	350 mV	-300e-3 < n < 900e-3
●	3.4	VRX-SE-max_n	369 mV	-300e-3 < n < 900e-3
●	3.6	VRX-CM	205 mV	120e-3 < n < 400e-3
●	3.7	VRX-CM-ACp-p	69.79 mV	<= 270.00 mV
●	3.2	VRX-IDLE-SE_p	5.9 mV	<= 75.0 mV
●	3.2	VRX-IDLE-SE_n	6.3 mV	<= 75.0 mV
●	3.1	VRX-DIFFp-p-min	453 mV	>= 170 mV
●	3.1	VRX-DIFFp-p-max	666 mV	<= 1.300 V
●	3.8	VRX-CM-EH-ratio	15.4029796485509	<=
●	3.5.1	TRX-Tj	0.14044373046875	<=
●	3.5.2	TRX-Dj	5.86144647848517E-03	<=
●	3.3	VRX-IDLE-DIFF-p-p	10.273 mV	<= 65.000 mV

Details

Test 1.2 - Single-ended maximum voltage

$V_{RefClk-max\_p}$

Single-ended maximum voltage on Refclk+

Pass

Limit Name: $V_{RefClk-max}$
Current Value: 799 mV
Test Criteria: <= 1.150 V
Timestamp: 2006/04/11 16:03:48

$V_{RefClk-max\_n}$

Single-ended maximum voltage on Refclk-

Pass

Limit Name: $V_{RefClk-max}$
Current Value: 821 mV
Test Criteria: <= 1.150 V
Timestamp: 2006/04/11 16:03:48

Test 1.3 - Single-ended minimum voltage

$V_{RefClk-min\_p}$

Single-ended minimum voltage on Refclk+

Pass

Limit Name: $V_{RefClk-min}$
Current Value: -14 mV
Test Criteria: >= -300 mV
Timestamp: 2006/04/11 16:03:48

$V_{RefClk-min\_n}$

Single-ended minimum voltage on Refclk-

Pass

Limit Name: $V_{RefClk-min}$
Current Value: -40 mV
Test Criteria: >= -300 mV
Timestamp: 2006/04/11 16:03:48

Test 1.4 - Absolute crossing point

$V_{RefClk-cross-min}$

Absolute Crossing Point - minimum

Pass

Limit Name: $V_{RefClk-cross-min}$
Current Value: 324.4 mV
Test Criteria: >= 250.0 mV
Timestamp: 2006/04/11 16:03:48

$V_{RefClk-cross-max}$

Absolute Crossing Point - maximum

Pass

Limit Name: $V_{RefClk-cross-max}$
Current Value: 371.5 mV

Test Criteria: <= 550.0 mV
Timestamp: 2006/04/11 16:03:49

Test 1.5 - VCross variation

$V_{RefClk\text{-}cross\text{-}delta}$

Vcross variation

Pass

Limit Name: $V_{RefClk\text{-}cross\text{-}delta}$
Current Value: 3.97009047739004E-02
Test Criteria: <=
Timestamp: 2006/04/11 16:03:49

Test 1.8 - % mismatch between rise and fall edge rates

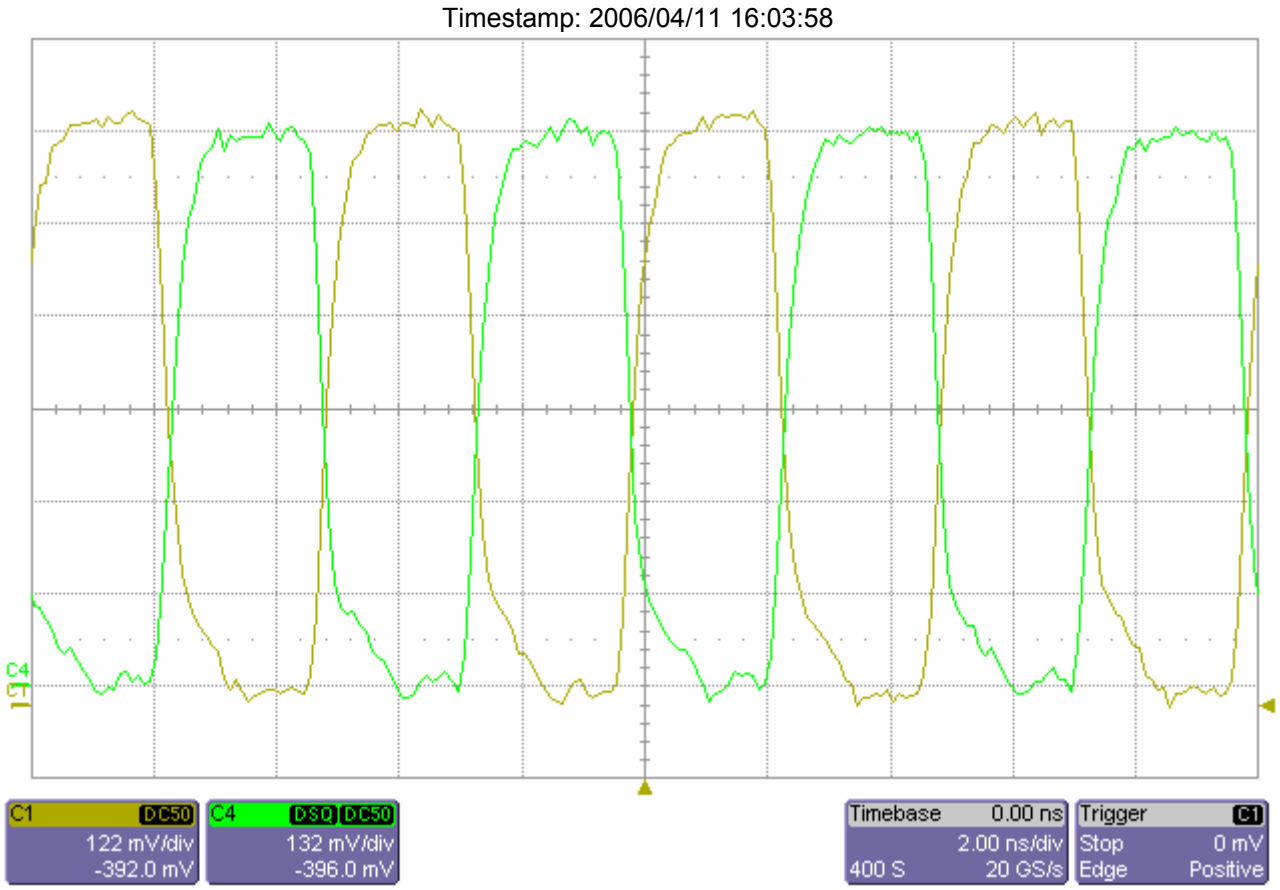
$ER_{RefClk\text{-}match}$

% mismatch between rise time on Refclk+ and fall time on Refclk-

Pass

Limit Name: $ER_{Refclk\text{-}Match}$
Current Value: 10.2999399960082
Test Criteria: <=
Timestamp: 2006/04/11 16:03:55

Figure 1.0 - Reference Clock Differential Single Lanes



Test 1.1 - Reference clock frequency

f_{RefClk}

Reference Clock Frequency

Pass

Limit Name: f_{Refclk}
Current Value: 200.056288 MHZ
Test Criteria: 190.00e6 < n < 200.10e6
Timestamp: 2006/04/11 16:04:17

Test 1.6 - Rising edge rate

$T_{RefClk-rise}$

Rising edge rate

Pass

Limit Name: $T_{Refclk-Rise}$
Current Value: 3.3187 GV/S
Test Criteria: 0.6e9 < n < 4.0e9
Timestamp: 2006/04/11 16:04:17

Test 1.7 - Falling edge rate

$T_{RefClk-fall}$

Falling edge rate

Pass

Limit Name: $T_{Refclk-Fall}$
Current Value: 3.0811 GV/S
Test Criteria: 0.6e9 < n < 4.0e9
Timestamp: 2006/04/11 16:04:17

Test 1.9 - Duty cycle of reference clock

$T_{RefClk-dutycycle}$

Duty Cycle of reference clock

Pass

Limit Name: $T_{Refclk-Dutycycle}$
Current Value: 49.29807 PCT
Test Criteria: 40 < n < 60
Timestamp: 2006/04/11 16:04:17

Test 1.10 - Reference clock jitter (rms), filtered

$T_{RefClk-jitter-rms}$

Reference clock jitter RMS filtered

Fail

Failure Explanation: cur [3.84302293172138E-12] is not <= ref [2.5e-12] (53.7209% error) keyword 0 numeric comparison failed
Limit Name: $T_{RefClk-jitter-rms}$
Current Value: 3.84 ps
Test Criteria: <= 2.50 ps
Timestamp: 2006/04/11 16:06:26

Figure 1.1 - Reference Clock Jitter Bathtub Curve

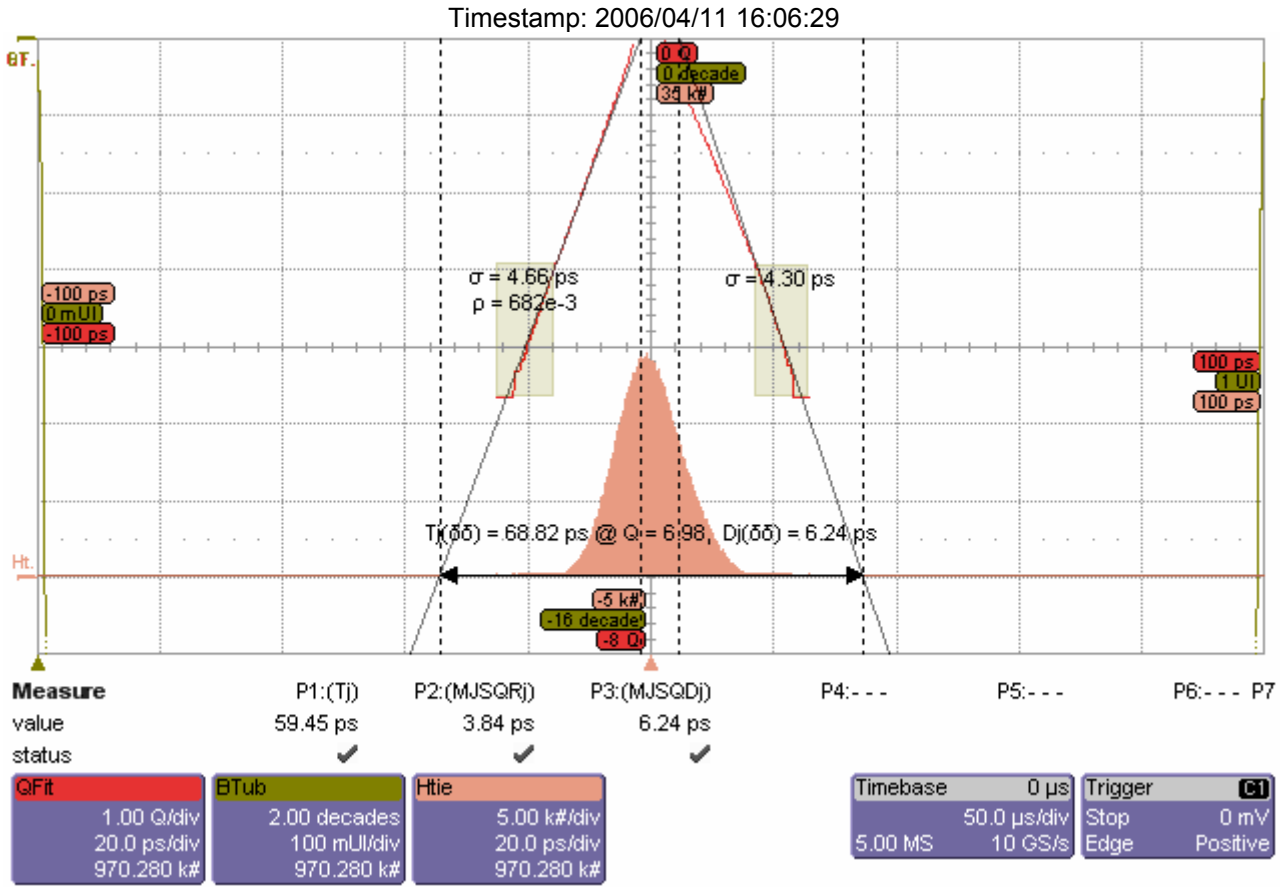
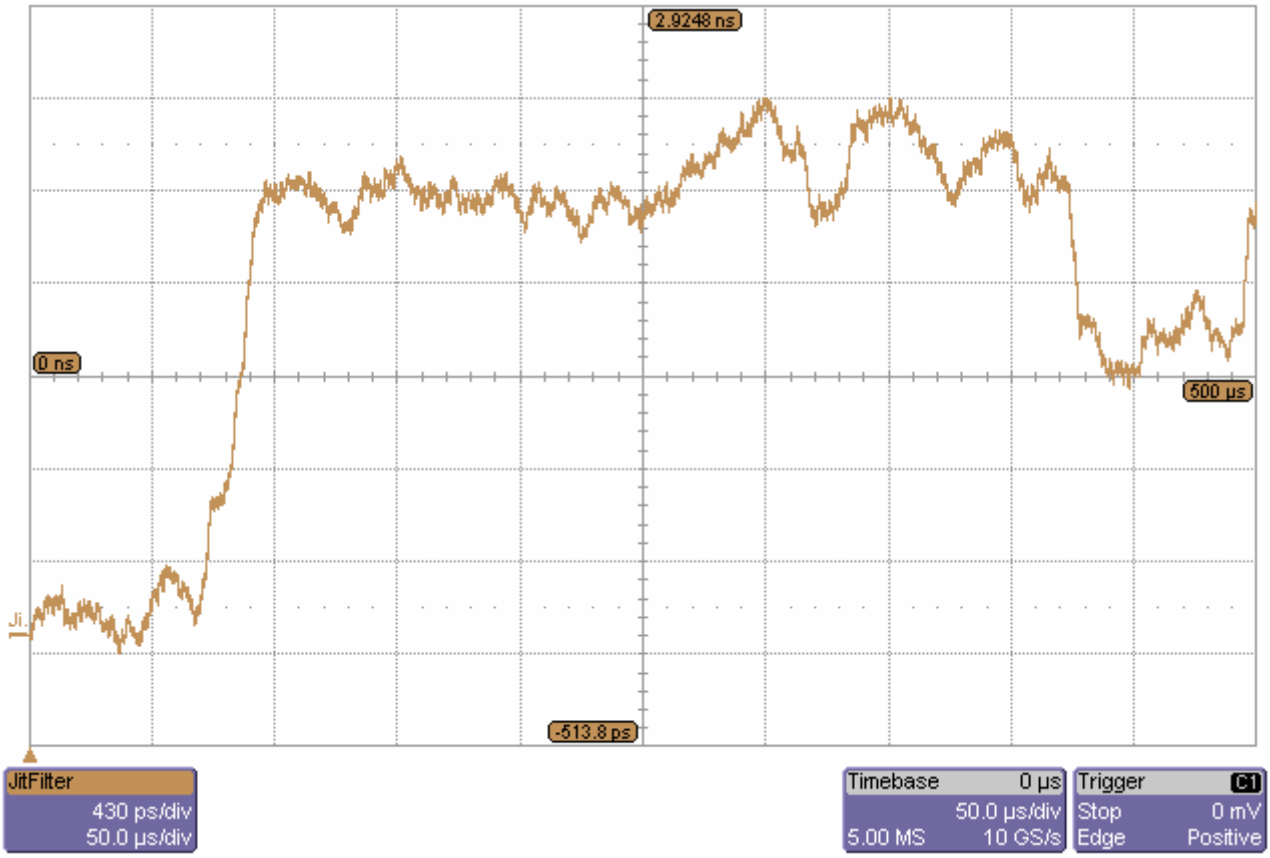


Figure 1.2 - Reference Clock SSC Track (PLL off)

Timestamp: 2006/04/11 16:06:33



Test 2.4 - DC common mode output voltage for large voltage swing

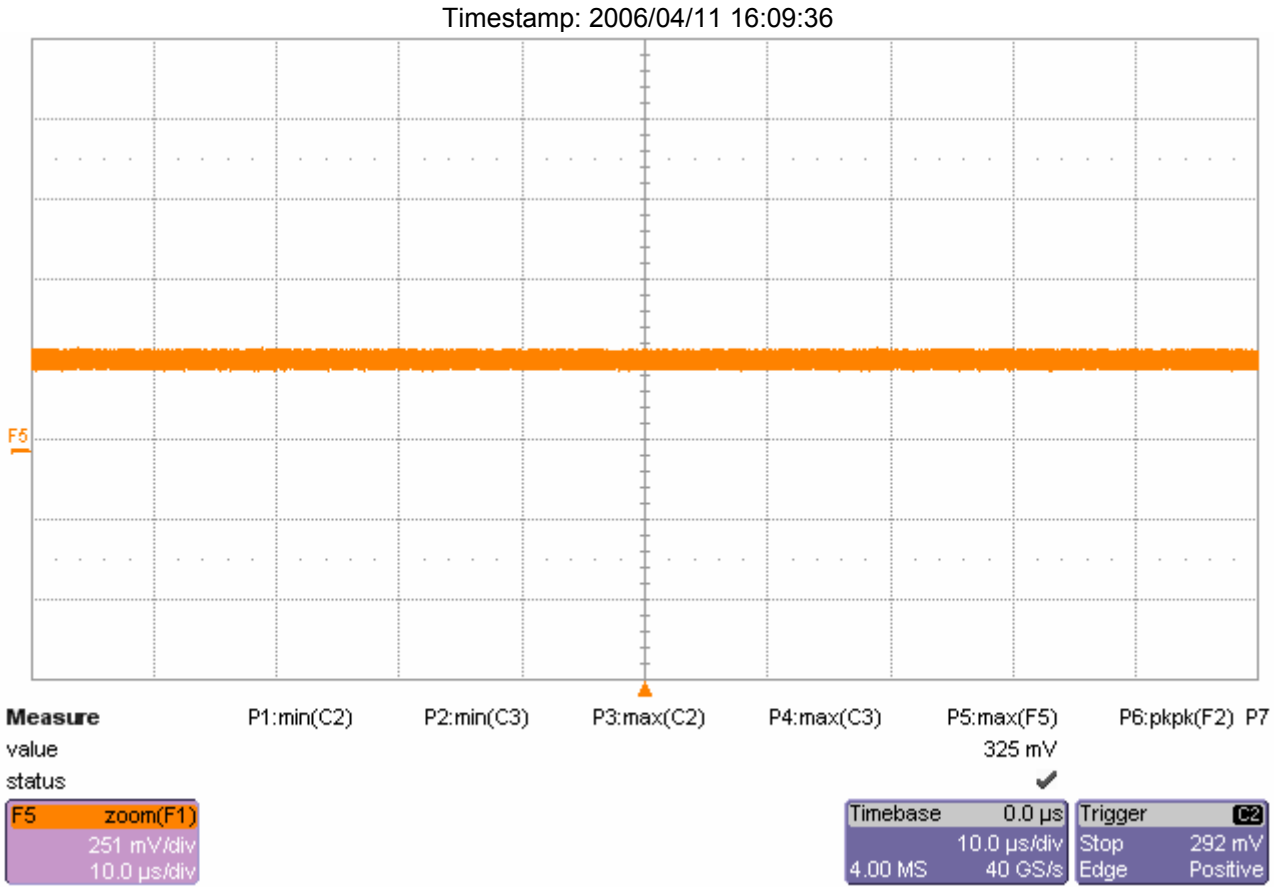
V_{TX-CM_L}

DC common mode output voltage for large voltage swing

Pass

Limit Name: V_{TX-CM_L}
Current Value: 325 mV
Test Criteria: <= 375 mV
Timestamp: 2006/04/11 16:09:34

Figure 2.4 - DC common mode for Large Voltage Swing.



Test 2.7 - AC peak-to-peak common mode output voltage for large voltage swing

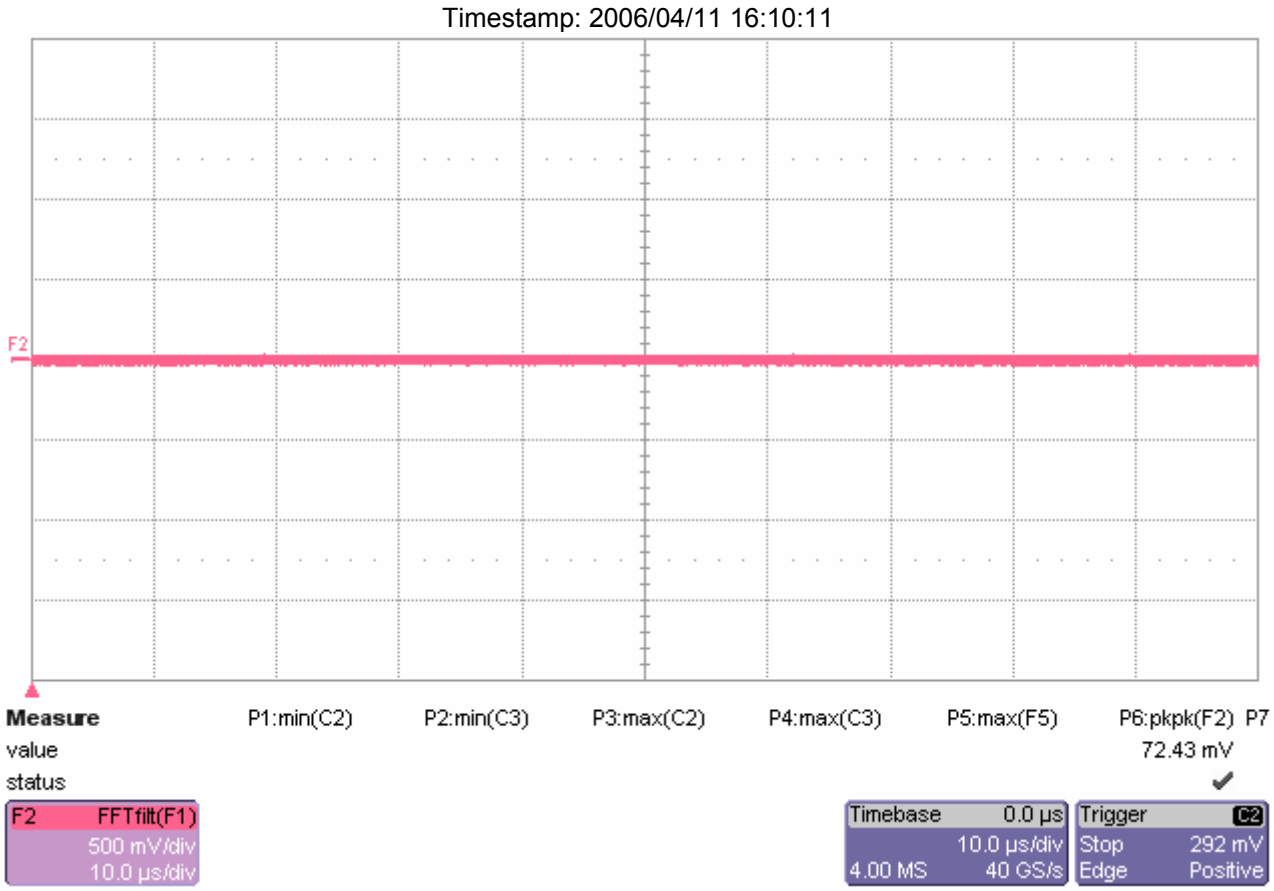
$V_{TX\text{-}CM\text{-}ACp\text{-}p\_L}$

AC peak-to-peak common mode output voltage for large voltage swing

Pass

Limit Name: $V_{TX\text{-}CM\text{-}ACp\text{-}p\_L}$
Current Value: 72.43 mV
Test Criteria: <= 90.00 mV
Timestamp: 2006/04/11 16:10:08

Figure 2.7 - AC Common Mode for Large Voltage Swing.



Test 2.13 - Single-ended voltage on D+/D-

$V_{TX-SE-min\_p}$

Minimum Single-ended voltage on Data+

Pass

Limit Name: V_{TX-SE}
Current Value: 55 mV
Test Criteria: -75e-3 < n < 750e-3
Timestamp: 2006/04/11 16:10:22

$V_{TX-SE-min\_n}$

Minimum Single-ended voltage on Data-

Pass

Limit Name: V_{TX-SE}
Current Value: 63 mV
Test Criteria: -75e-3 < n < 750e-3
Timestamp: 2006/04/11 16:10:22

$V_{TX-SE-max\_p}$

Maximum Single-ended voltage on Data+

Pass

Limit Name: V_{TX-SE}
Current Value: 522 mV
Test Criteria: -75e-3 < n < 750e-3
Timestamp: 2006/04/11 16:10:22

$V_{TX-SE-max\_n}$

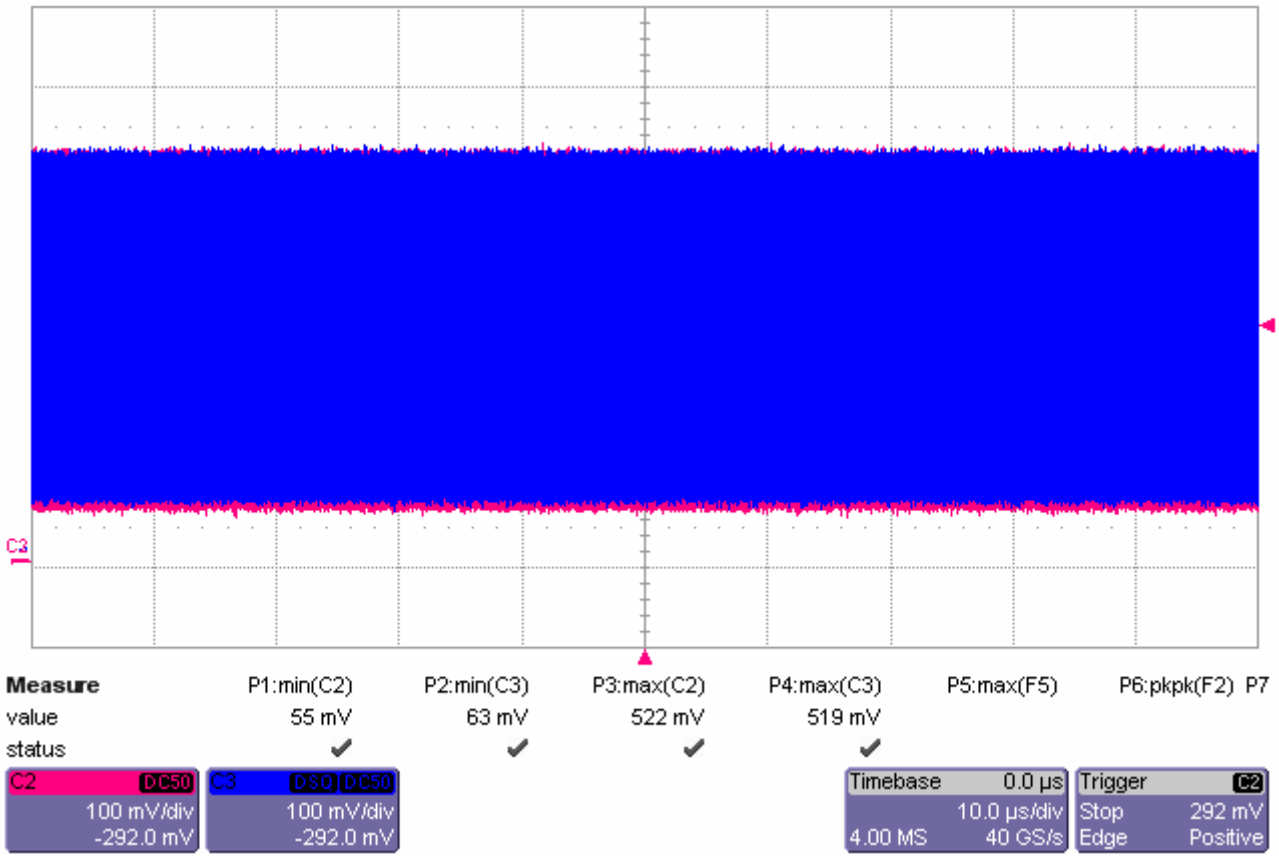
Maximum Single-ended voltage on Data-

Pass

Limit Name: V_{TX-SE}
Current Value: 519 mV
Test Criteria: -75e-3 < n < 750e-3
Timestamp: 2006/04/11 16:10:22

Figure 2.13 - Single-Ended voltage

Timestamp: 2006/04/11 16:10:25



Test 2.8 - AC peak-to-peak common mode output voltage for regular voltage swing

$V_{TX\text{-}CM\text{-}ACp\text{-}p\_R}$

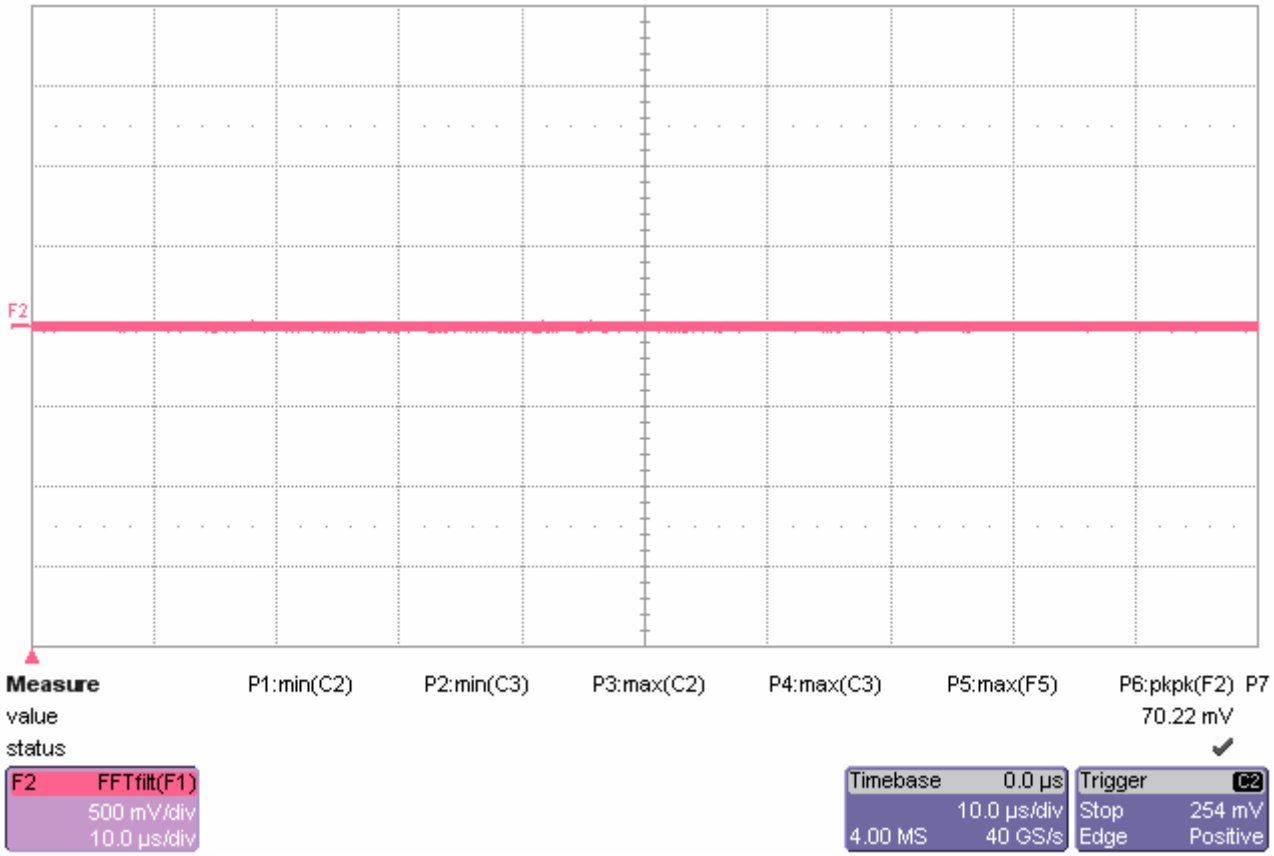
AC peak-to-peak common mode output voltage for regular voltage swing

Pass

Limit Name: $V_{TX\text{-}CM\text{-}ACp\text{-}p\_R}$
Current Value: 70.22 mV
Test Criteria: <= 80.00 mV
Timestamp: 2006/04/11 16:11:55

Figure 2.8 - AC Common Mode for Regular Voltage Swing.

Timestamp: 2006/04/11 16:11:57



Test 2.5 - DC common mode output voltage for small voltage swing

$V_{TX\text{-}CM\_S}$

DC common mode output voltage for small voltage swing

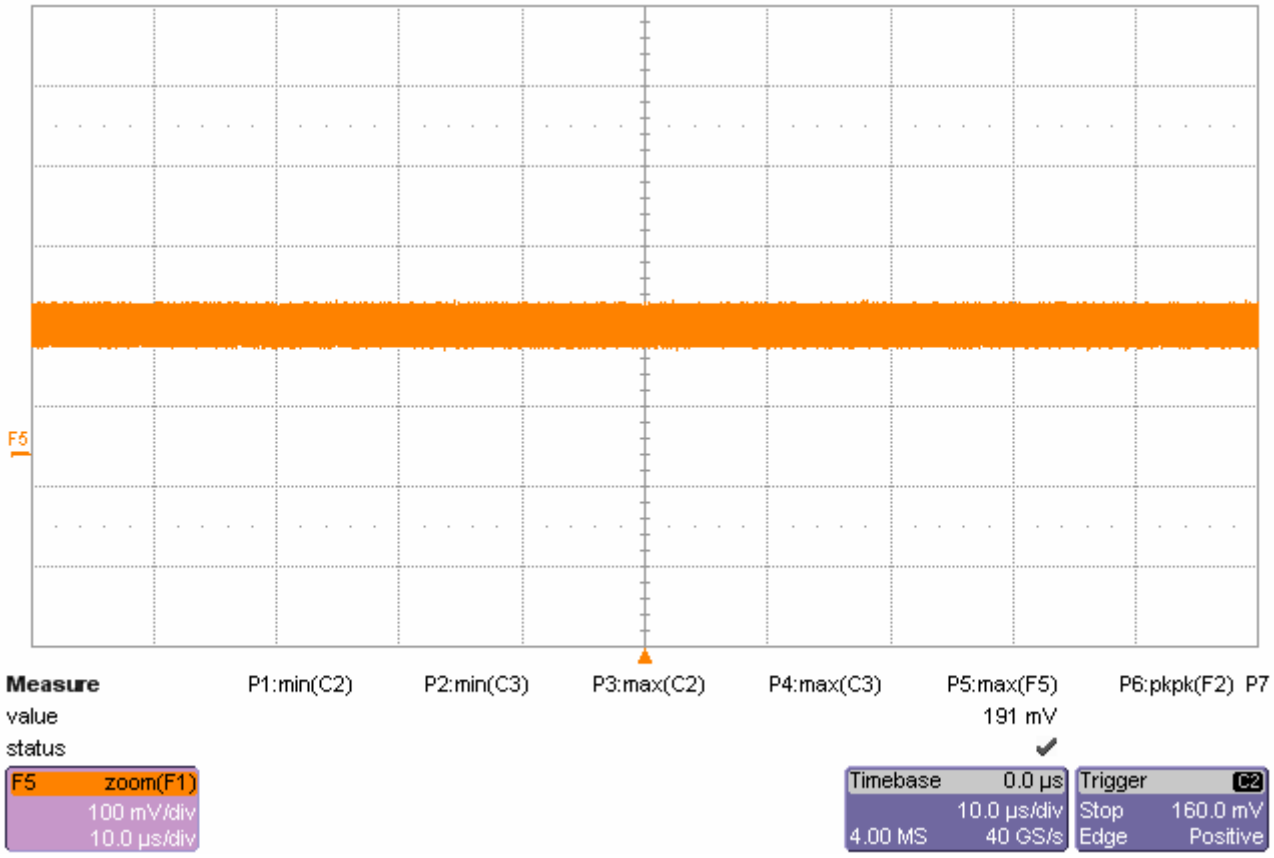
Pass

Limit Name: $V_{TX\text{-}CM\_S}$
Current Value: 191 mV
Test Criteria: 135e-3 < n < 280e-3

Timestamp: 2006/04/11 16:13:16

Figure 2.4 - DC Common Mode for Large Voltage Swing.

Timestamp: 2006/04/11 16:13:19



Test 2.9 - AC peak-to-peak common mode output voltage for small voltage swing

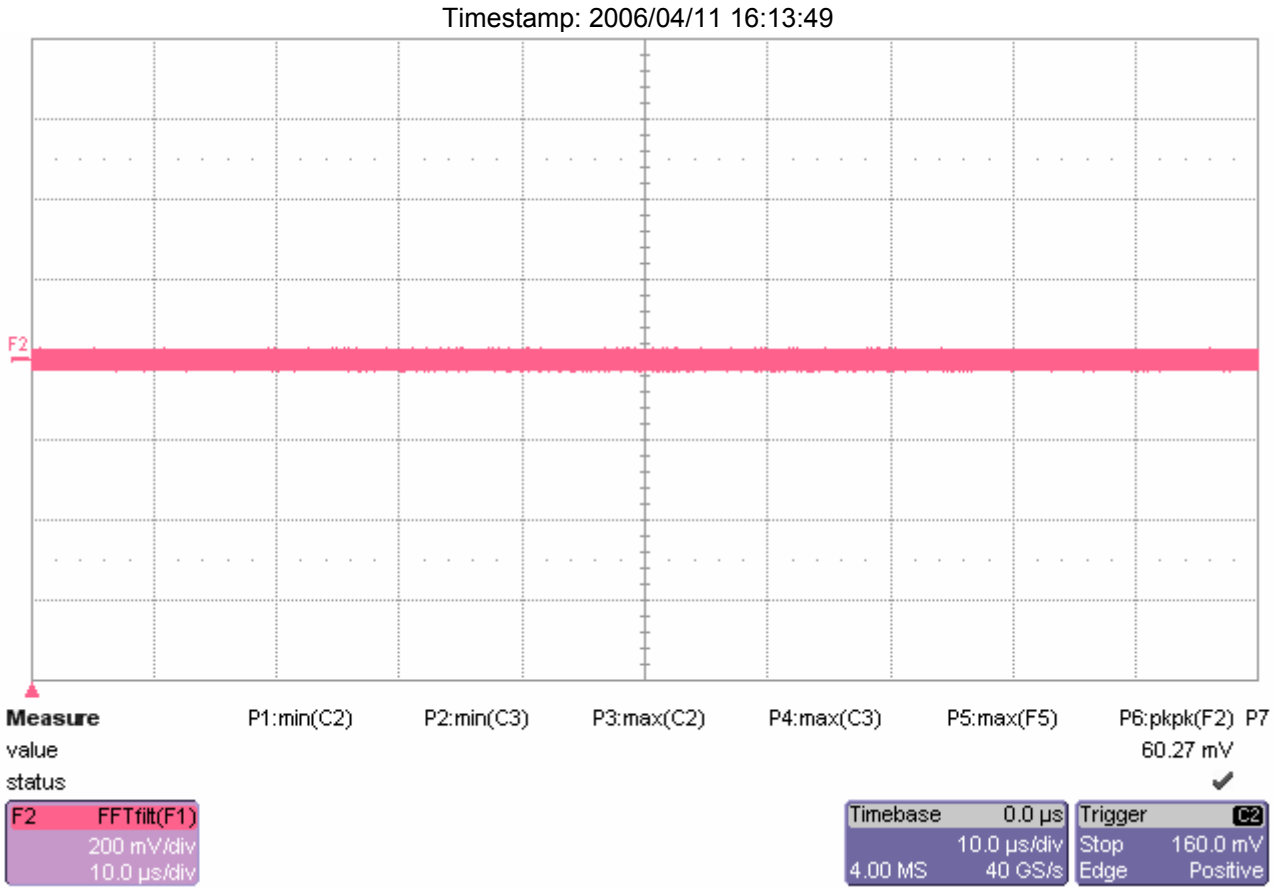
$V_{TX\text{-}CM\text{-}ACp\text{-}p\_S}$

AC peak-to-peak common mode output voltage for small voltage swing

Pass

Limit Name: $V_{TX\text{-}CM\text{-}ACp\text{-}p\_S}$
Current Value: 60.27 mV
Test Criteria: <= 70.00 mV
Timestamp: 2006/04/11 16:13:47

Figure 2.9 - AC Common Mode for Small Voltage Swing.



Test 2.10 - Maximum single-ended voltage in EI condition, DC + AC

$V_{TX-IDLE-SE\_p}$

Maximum single-ended voltage in EI condition, DC + AC on Data+

Pass

Limit Name: $V_{TX-IDLE-SE}$
Current Value: 7.7 mV
Test Criteria: <= 50.0 mV
Timestamp: 2006/04/11 16:15:03

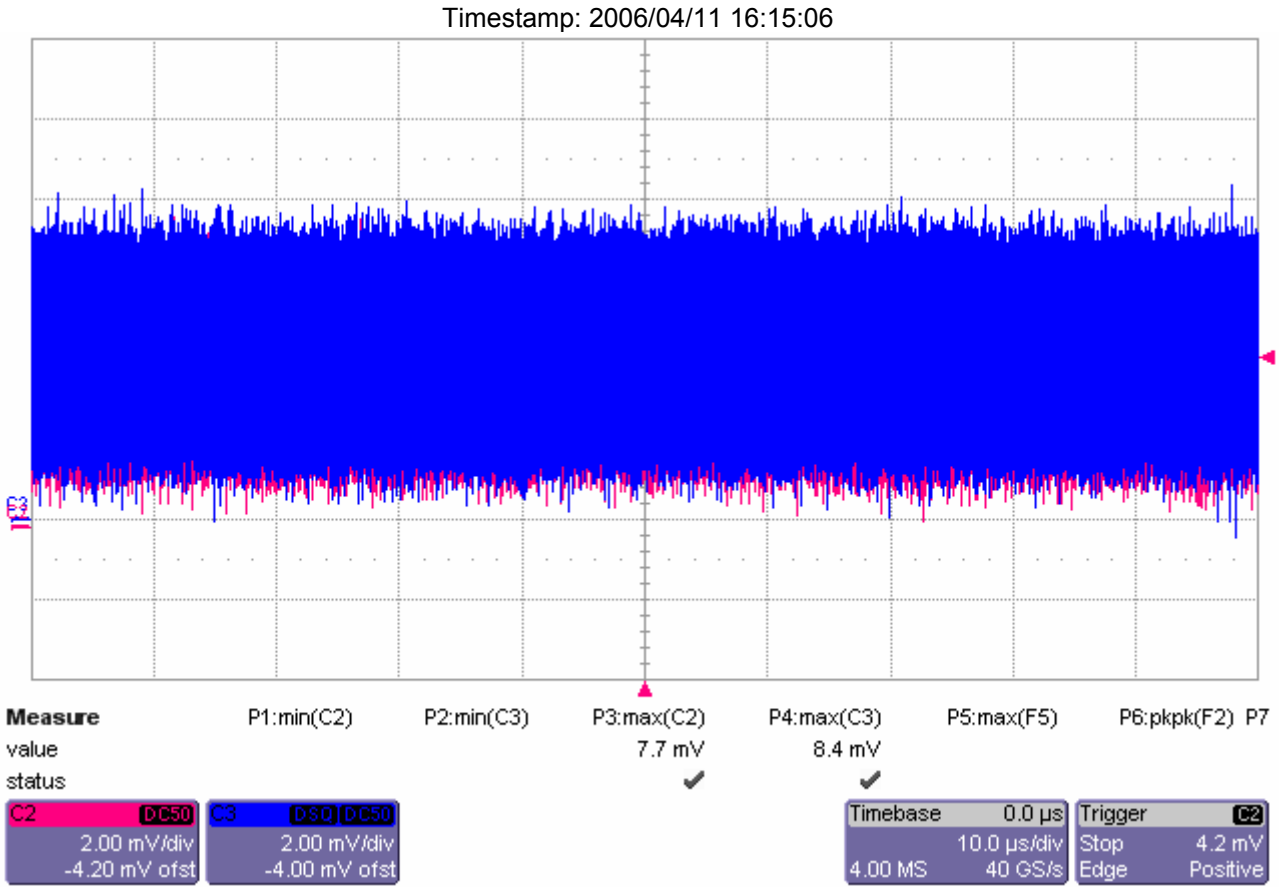
$V_{TX-IDLE-SE\_n}$

Maximum single-ended voltage in EI condition, DC + AC on Data-

Pass

Limit Name: $V_{TX-IDLE-SE}$
Current Value: 8.4 mV
Test Criteria: <= 50.0 mV
Timestamp: 2006/04/11 16:15:03

Figure 2.11 - Maximum Single-ended Voltage in EI Condition (DC only)



Test 2.11 - Maximum single-ended voltage in EI condition, DC only

$V_{TX\text{-}IDLE\text{-}SE\text{-}DC\_p}$

Maximum single-ended voltage in EI condition, DC only on Data+

Pass

Limit Name: $V_{TX\text{-}IDLE\text{-}SE\text{-}DC}$
Current Value: 7.7 mV
Test Criteria: <= 20.0 mV
Timestamp: 2006/04/11 16:15:16

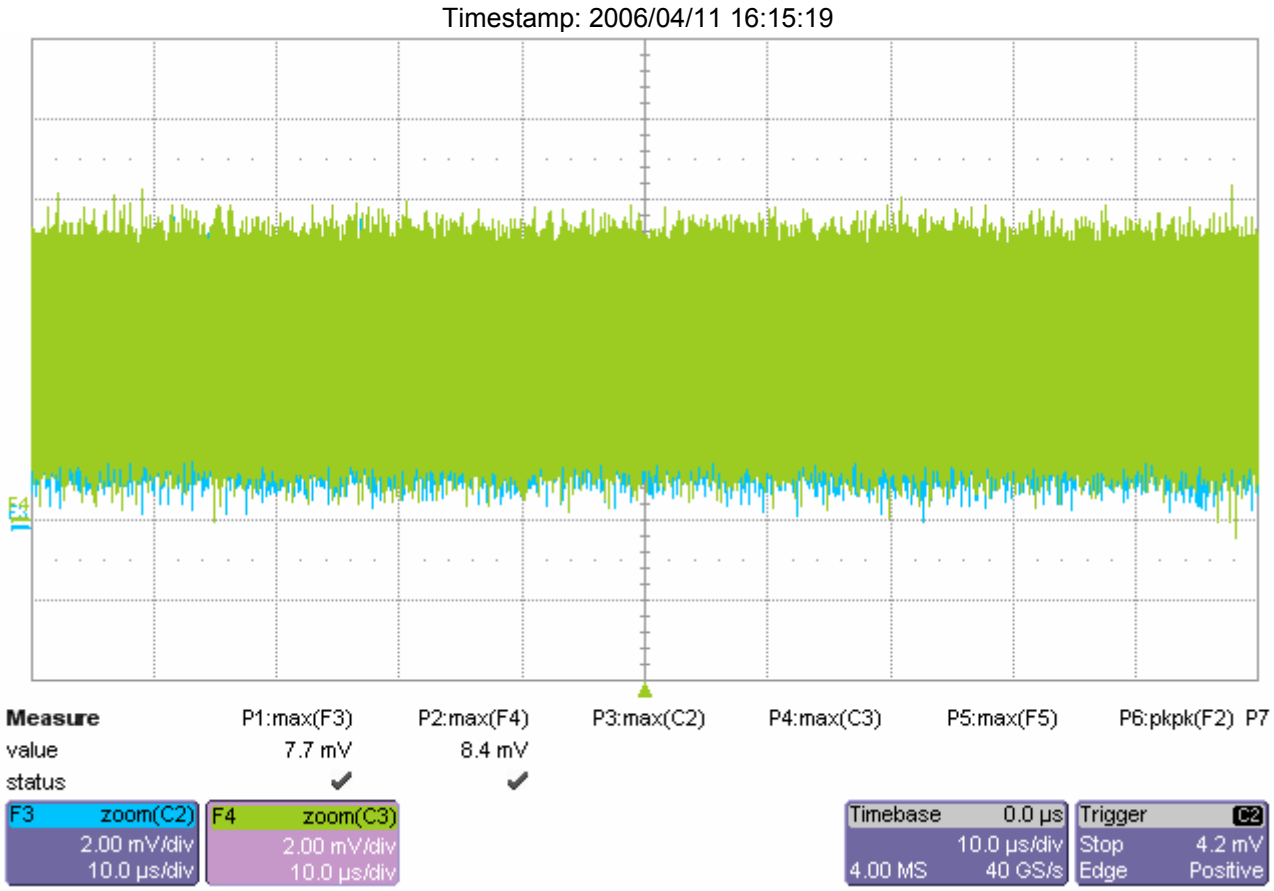
$V_{TX\text{-}IDLE\text{-}SE\text{-}DC\_n}$

Maximum single-ended voltage in EI condition, DC only on Data-

Pass

Limit Name: $V_{TX\text{-}IDLE\text{-}SE\text{-}DC}$
Current Value: 8.4 mV
Test Criteria: <= 20.0 mV
Timestamp: 2006/04/11 16:15:16

Figure 2.10 - Maximum Single-ended Voltage in EI Condition (AC + DC)



Test 2.1 - Differential peak-to-peak output voltage for large voltage swing

$V_{TX-DIFFp-p\_L-min}$

Differential peak-to-peak output voltage for large voltage swing - minimum

Fail

Failure Explanation: cur [0.718585772594301] is not >= ref [900e-3] (20.1571% error) keyword 0 numeric comparison failed
Limit Name: $V_{TX-DIFFp-p\_L-min}$
Current Value: 719 mV
Test Criteria: >= 900 mV
Timestamp: 2006/04/11 16:27:09

$V_{TX-DIFFp-p\_L-max}$

Differential peak-to-peak output voltage for large voltage swing - maximum

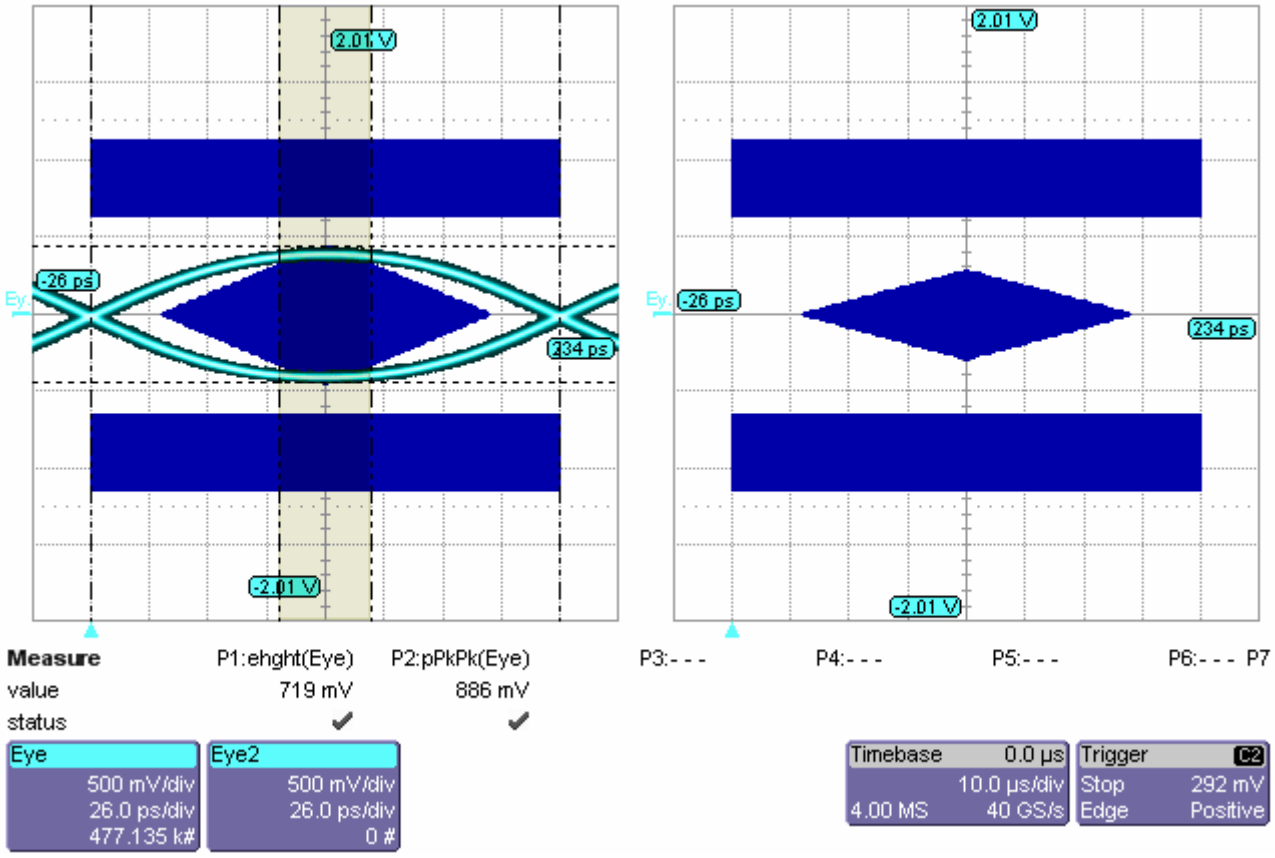
Pass

Limit Name: $V_{TX-DIFFp-p\_L-max}$
Current Value: 886 mV
Test Criteria: <= 1.300 V

Timestamp: 2006/04/11 16:27:09

Figure 2.1 - Differential Pk-Pk Output Voltage for Large Voltage Swing.

Timestamp: 2006/04/11 16:27:12



Test 2.2 - Differential peak-to-peak output voltage for regular voltage swing

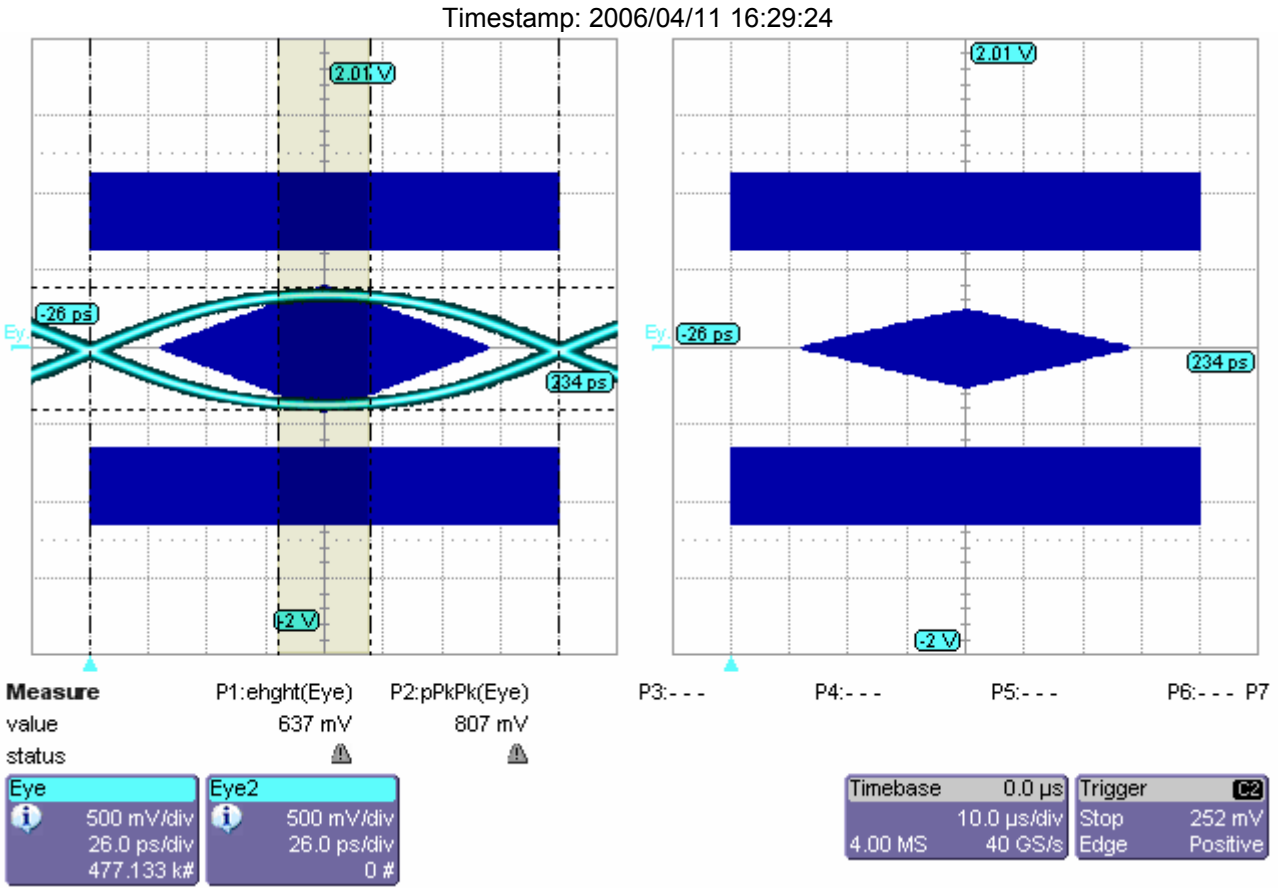
$V_{TX-DIFFp-p\_R-min}$

Differential peak-to-peak output voltage for regular voltage swing - minimum

Fail

Failure Explanation: cur [0.637082930231869] is not >= ref [800e-3] (20.3646% error) keyword 0 numeric comparison failed
Limit Name: $V_{TX-DIFFp-p\_R-min}$
Current Value: 637 mV
Test Criteria: >= 800 mV
Timestamp: 2006/04/11 16:29:21

Figure 2.2 - Differential Pk-Pk Output Voltage for Regular Voltage Swing.



Test 2.3 - Differential peak-to-peak output voltage for regular small swing

$V_{TX-DIFFp-p\_S-min}$

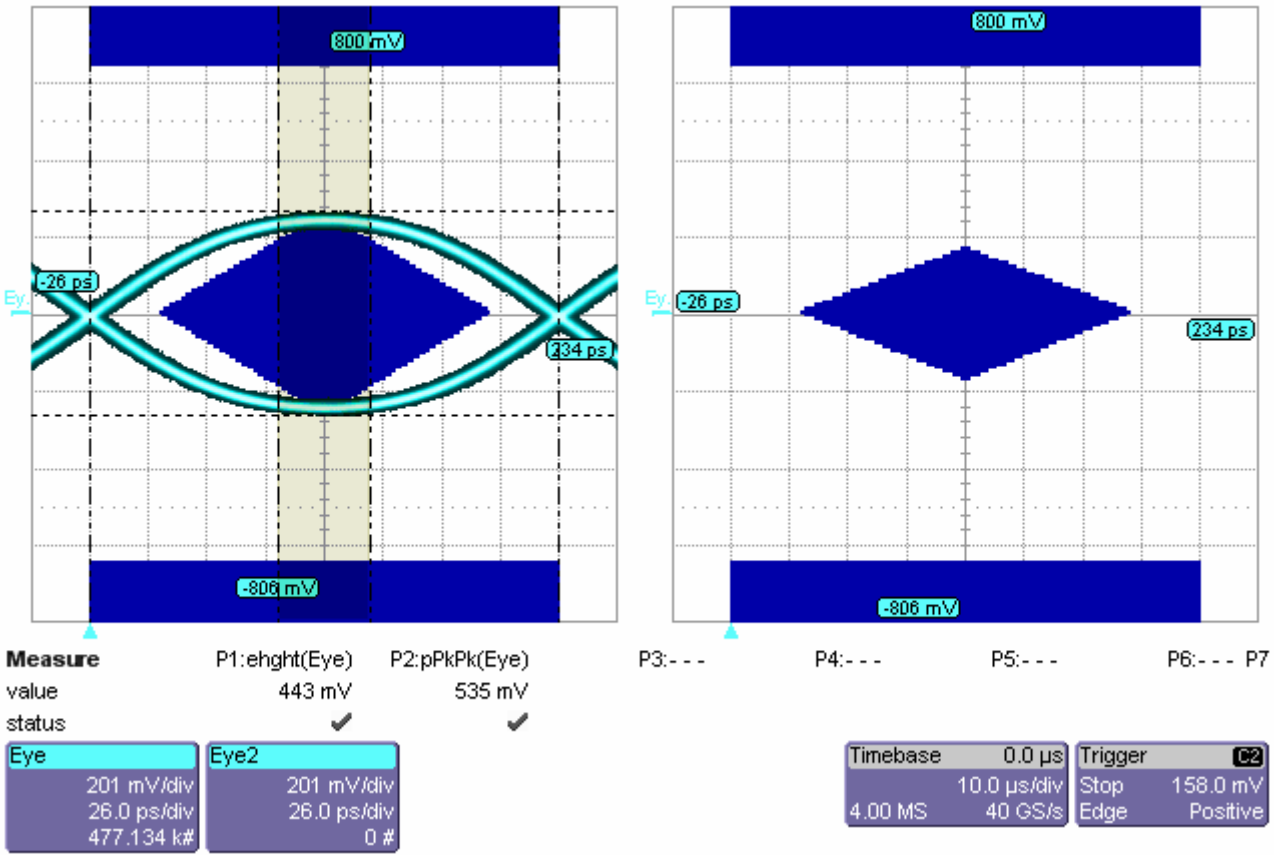
Differential peak-to-peak output voltage for regular small swing - minimum

Fail

Failure Explanation: cur [0.442725111570617] is not >= ref [520e-3] (14.8605% error) keyword 0 numeric comparison failed
Limit Name: $V_{TX-DIFFp-p\_S-min}$
Current Value: 443 mV
Test Criteria: >= 520 mV
Timestamp: 2006/04/11 16:32:26

Figure 2.3 - Differential Pk-Pk Output Voltage for Small Voltage Swing.

Timestamp: 2006/04/11 16:32:29



Test 2.14 - Minimum TX eye width

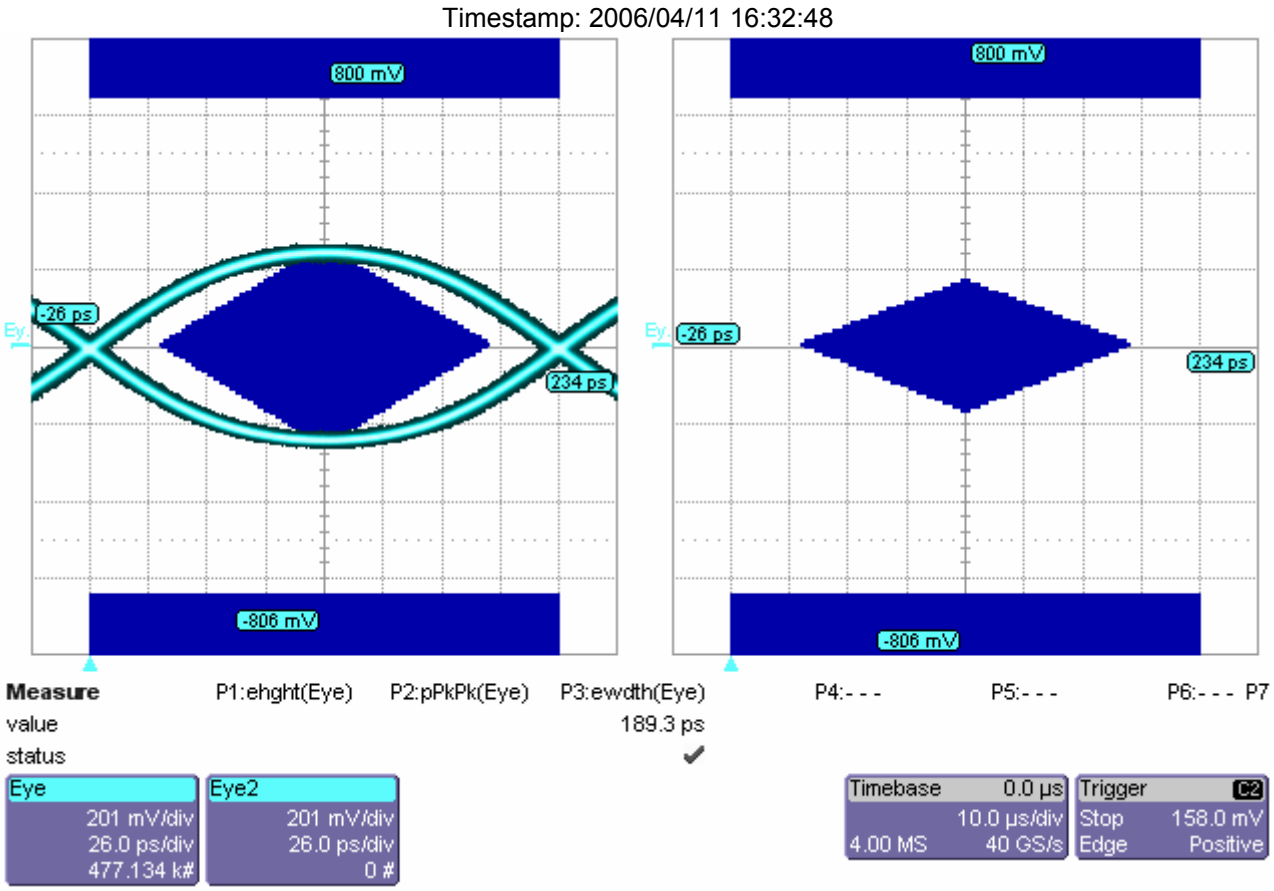
$T_{TX\text{-}eye\text{-}min}$

Minimum TX Eye Width

Pass

Limit Name: $T_{TX\text{-}EYE\text{-}MIN}$
Current Value: 0.908850927739682
Test Criteria: >=
Timestamp: 2006/04/11 16:32:46

Figure 2.14 - Maximum TX Eye Width



Test 2.17 - Differential TX output rise time

$T_{TX\text{-}rise}$

Differential TX output Rise

Pass

Limit Name: $T_{TX\text{-}RISE}$
Current Value: 74.428 ps
Test Criteria: 30e-12 < n < 90e-12
Timestamp: 2006/04/11 16:33:02

Test 2.18 - Differential TX output fall time

$T_{TX\text{-}fall}$

Differential TX output Fall

Pass

Limit Name: $T_{TX\text{-}FALL}$
Current Value: 74.664 ps
Test Criteria: 30e-12 < n < 90e-12
Timestamp: 2006/04/11 16:33:02

Test 2.19 - Mismatch between rise and fall times

$T_{TX\text{-}RF\text{-}mismatch}$

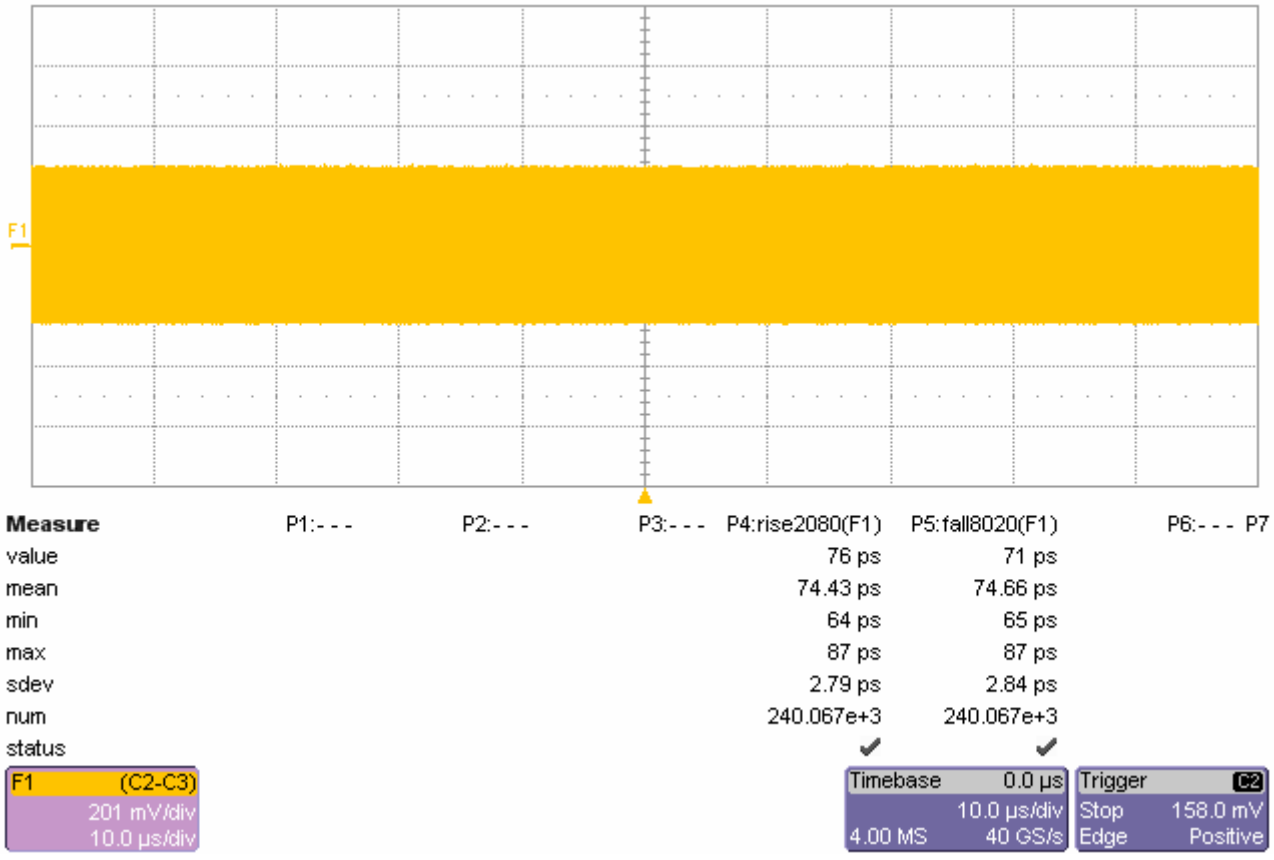
Mismatch between rise and fall times

Pass

Limit Name: $T_{TX\text{-}RF\text{-}MISMATCH}$
Current Value: 2.36552061137673E-13
Test Criteria: <=
Timestamp: 2006/04/11 16:33:02

Figure 2.17 - Rise and Fall Time Measurements.

Timestamp: 2006/04/11 16:33:05



Test 2.6.1 - De-emphasized differential output voltage ratio for -3.5 dB de-emphasis

$V_{TX\text{-}DE\text{-}3.5\text{-}ratio}$

De-emphasized differential output voltage ratio for -3.5dB de-emphasis

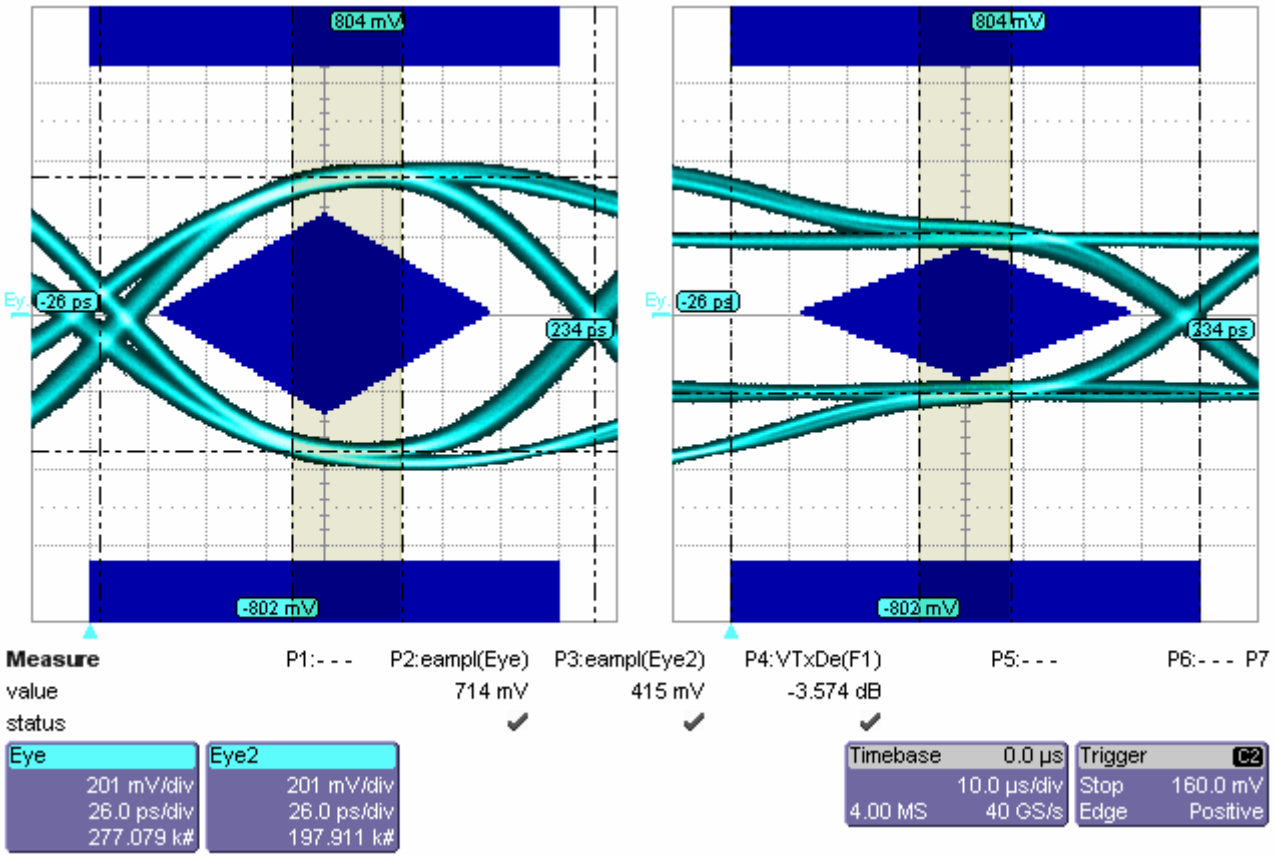
Fail

Failure Explanation: Current value -4.71406 outside the Limit VTX-DE-3.5-Ratio Lower limit: -3, Upper limit: -4 Within limit test failed
Limit Name: VTX-DE-3.5-Ratio
Current Value: -4.71406087786773

Test Criteria: -3 < n < -4
Timestamp: 2006/04/11 16:35:57

Figure 2.6.1 - TX De-emphasis -3.5 dB Ratio

Timestamp: 2006/04/11 16:36:00



Test 2.6.2 - De-emphasized differential output voltage ratio for -6 dB de-emphasis

$V_{TX-DE-6-ratio}$

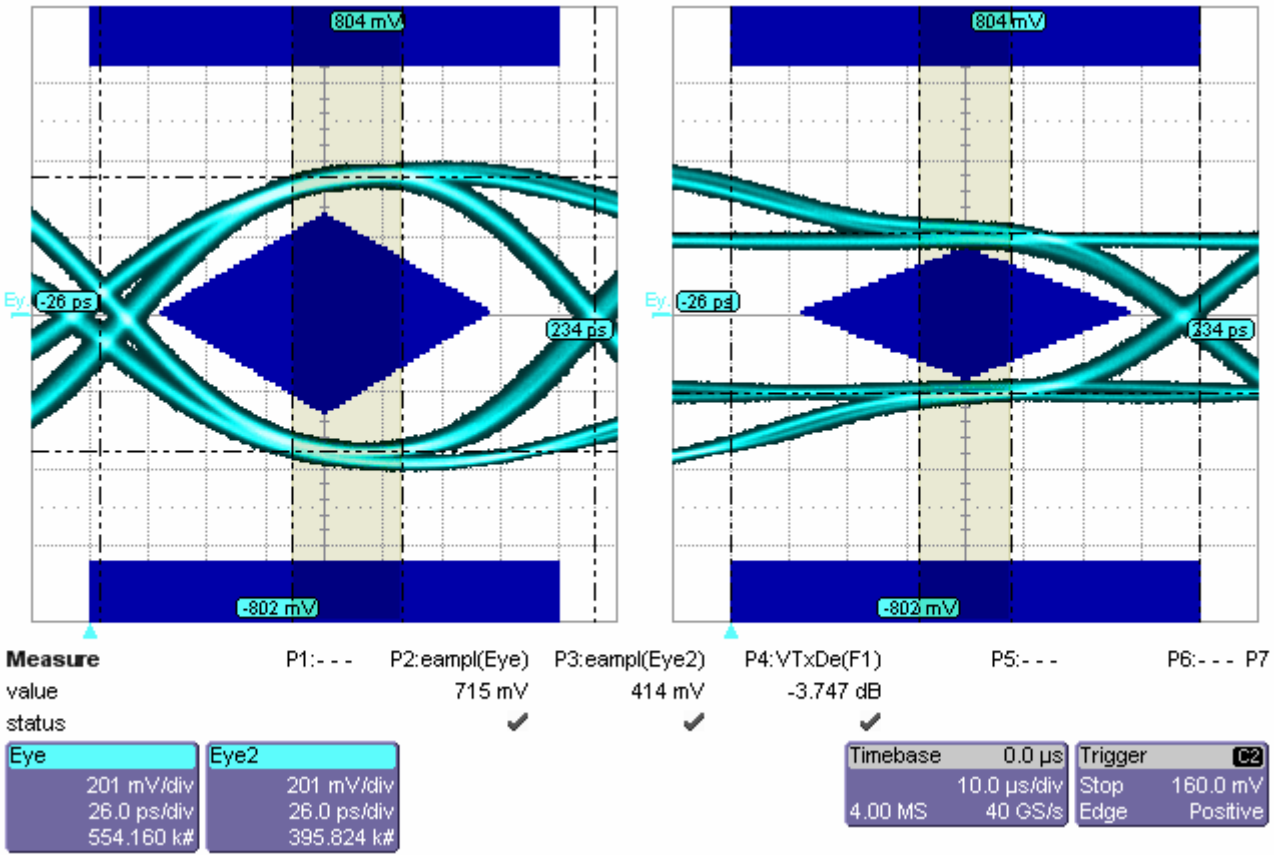
De-emphasized differential output voltage ratio for -6dB de-emphasis

Fail

Failure Explanation: Current value -4.74736 outside the Limit VTX-DE-6.0-Ratio Lower limit: -5, Upper limit: -7 Within limit test failed
Limit Name: $V_{TX-DE-6.0-Ratio}$
Current Value: -4.7473631144758
Test Criteria: -5 < n < -7
Timestamp: 2006/04/11 16:36:59

Figure 2.6.2 - TX De-emphasis -6 dB Ratio

Timestamp: 2006/04/11 16:37:02



Test 2.16 - Instantaneous pulse width

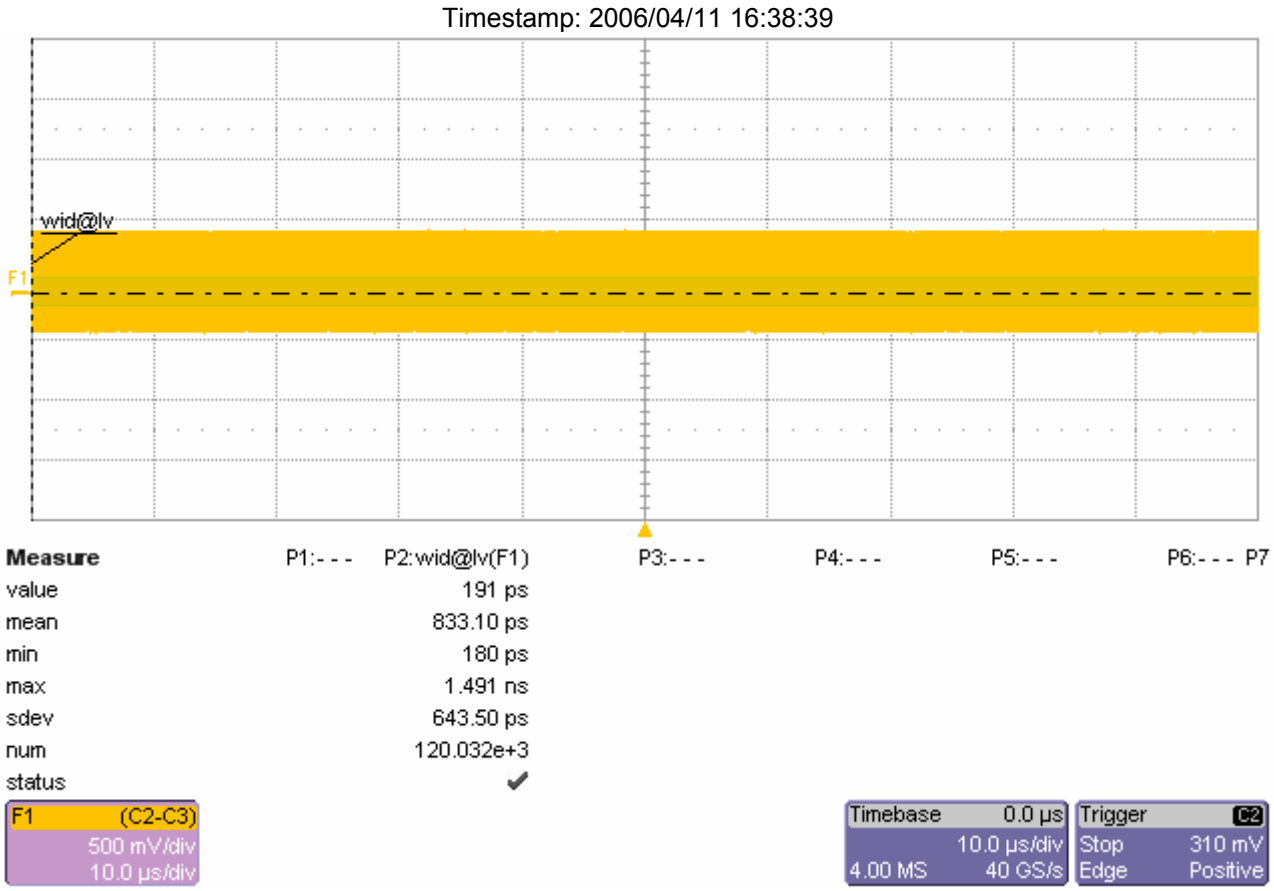
$T_{TX\text{-}pulse}$

Minimum pulse width

Pass

Limit Name: $T_{TX\text{-}PULSE}$
Current Value: 0.863380579790157
Test Criteria: >=
Timestamp: 2006/04/11 16:38:37

Figure 2.16 - TX Instantaneous Pulse Width



Test 2.15 - Maximum TX deterministic jitter

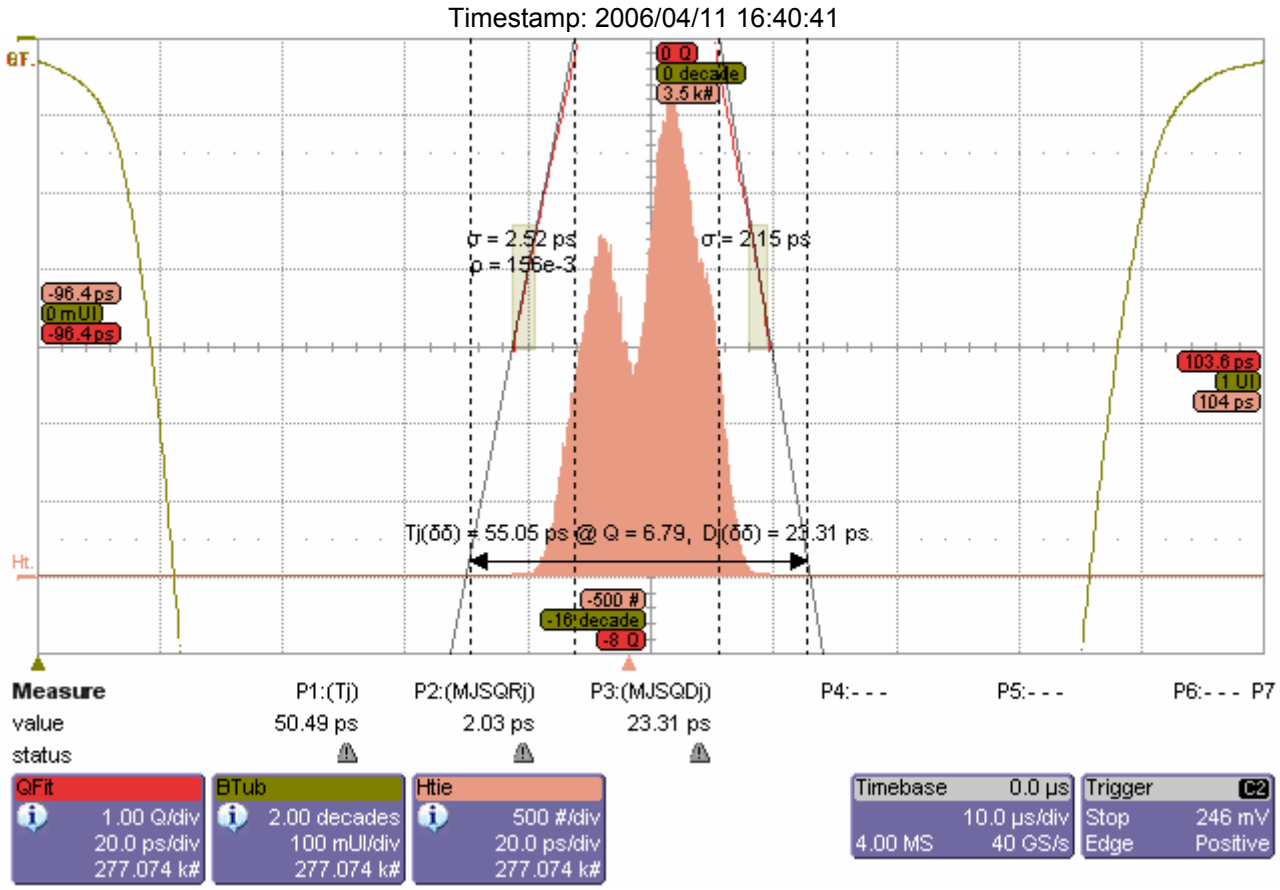
T_{TX-Dj}

TX - Deterministic Jitter

Pass

Limit Name: T_{TX-Dj}
Current Value: 0.111908040420286
Test Criteria: <=
Timestamp: 2006/04/11 16:40:40

Figure 1.1 - Reference Clock Jitter Bathtub Curve



Test 2.12 - Maximum peak-to-peak differential voltage in EI condition

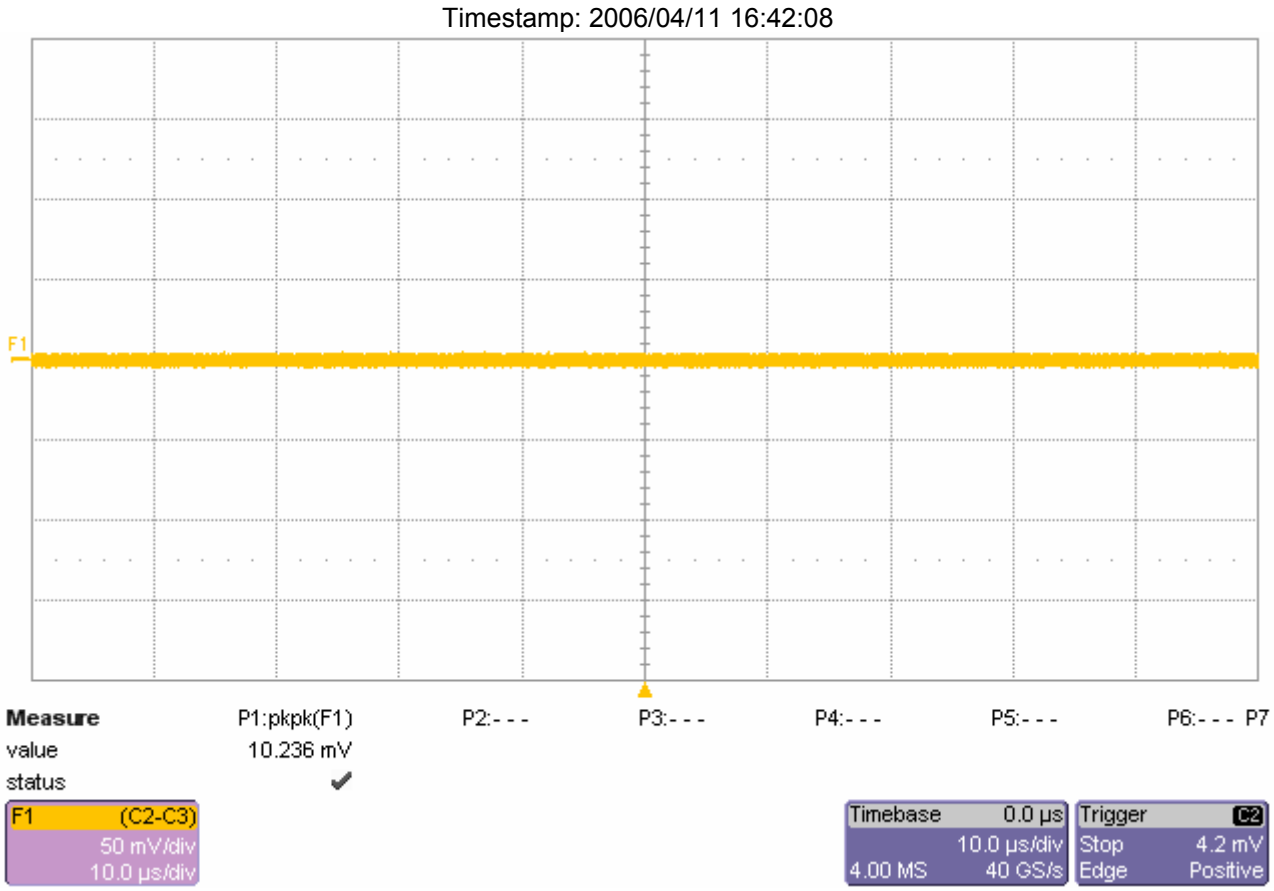
$V_{TX-IDLE-DIFFp-p}$

Maximum peak-to-peak differential voltage in EI condition

Pass

Limit Name: $V_{TX-IDLE-DIFFp-p}$
Current Value: 10.236 mV
Test Criteria: <= 40.000 mV
Timestamp: 2006/04/11 16:42:05

Figure 2.12 - Maximum Pk-Pk Differential Voltage in EI Condition.



Test 3.4 - Single-ended voltage on D+/D-

$V_{RX-SE-min\_p}$

Minimum Single-ended voltage (w.r.t. VSS) on Data+

Pass

Limit Name: V_{RX-SE}
Current Value: 1 mV
Test Criteria: -300e-3 < n < 900e-3
Timestamp: 2006/04/11 16:45:34

$V_{RX-SE-min\_n}$

Minimum Single-ended voltage (w.r.t. VSS) on Data-

Pass

Limit Name: V_{RX-SE}
Current Value: -4 mV
Test Criteria: -300e-3 < n < 900e-3
Timestamp: 2006/04/11 16:45:34

$V_{RX-SE-max\_p}$

Maximum Single-ended voltage (w.r.t. VSS) on Data+

Pass

Limit Name: V_{RX-SE}
Current Value: 324 mV
Test Criteria: -300e-3 < n < 900e-3
Timestamp: 2006/04/11 16:45:34

$V_{RX-SE-max\_n}$

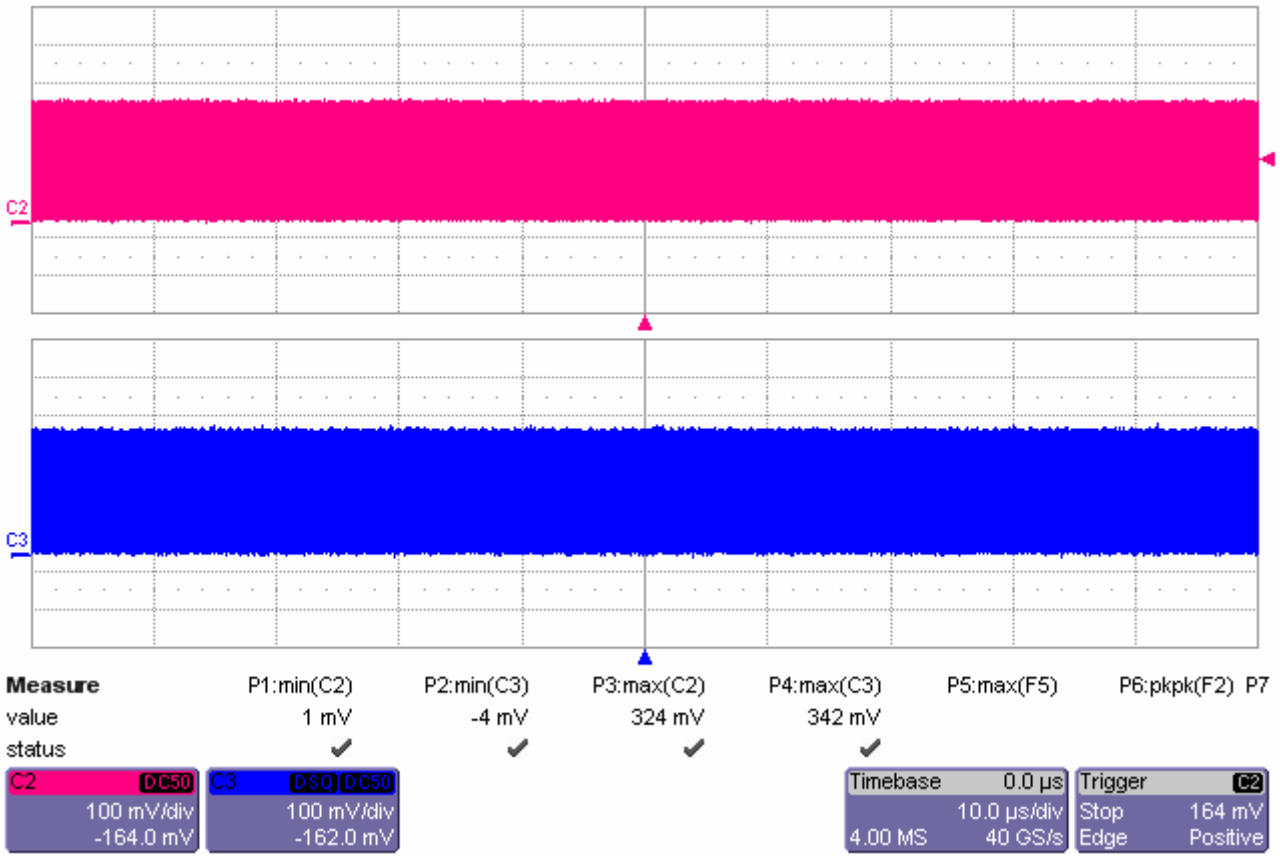
Maximum Single-ended voltage (w.r.t. VSS) on Data-

Pass

Limit Name: V_{RX-SE}
Current Value: 342 mV
Test Criteria: -300e-3 < n < 900e-3
Timestamp: 2006/04/11 16:45:34

Figure 3.4 - RX Single-Ended Voltage

Timestamp: 2006/04/11 16:45:36



Test 3.6 - Common mode of the input voltage (DC average)

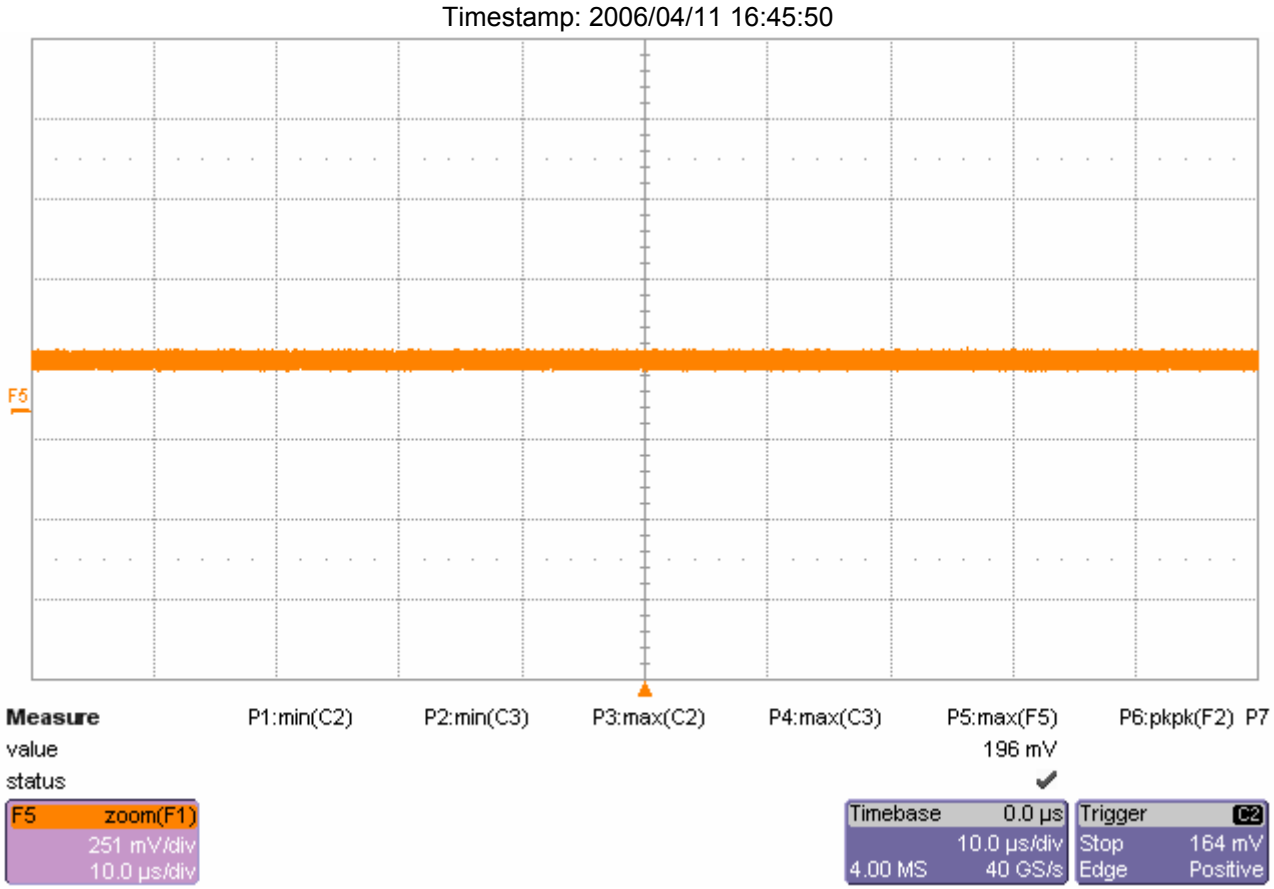
V_{RX-CM}

Common mode of the input voltage (DC average)

Pass

Limit Name: V_{RX-CM}
Current Value: 196 mV
Test Criteria: 120e-3 < n < 400e-3
Timestamp: 2006/04/11 16:45:47

Figure 3.6 - RX DC Common Mode Voltage.



Test 3.7 - AC peak-to-peak common mode input voltage

$V_{RX-CM-ACp-p}$

AC peak-to-peak common mode input voltage

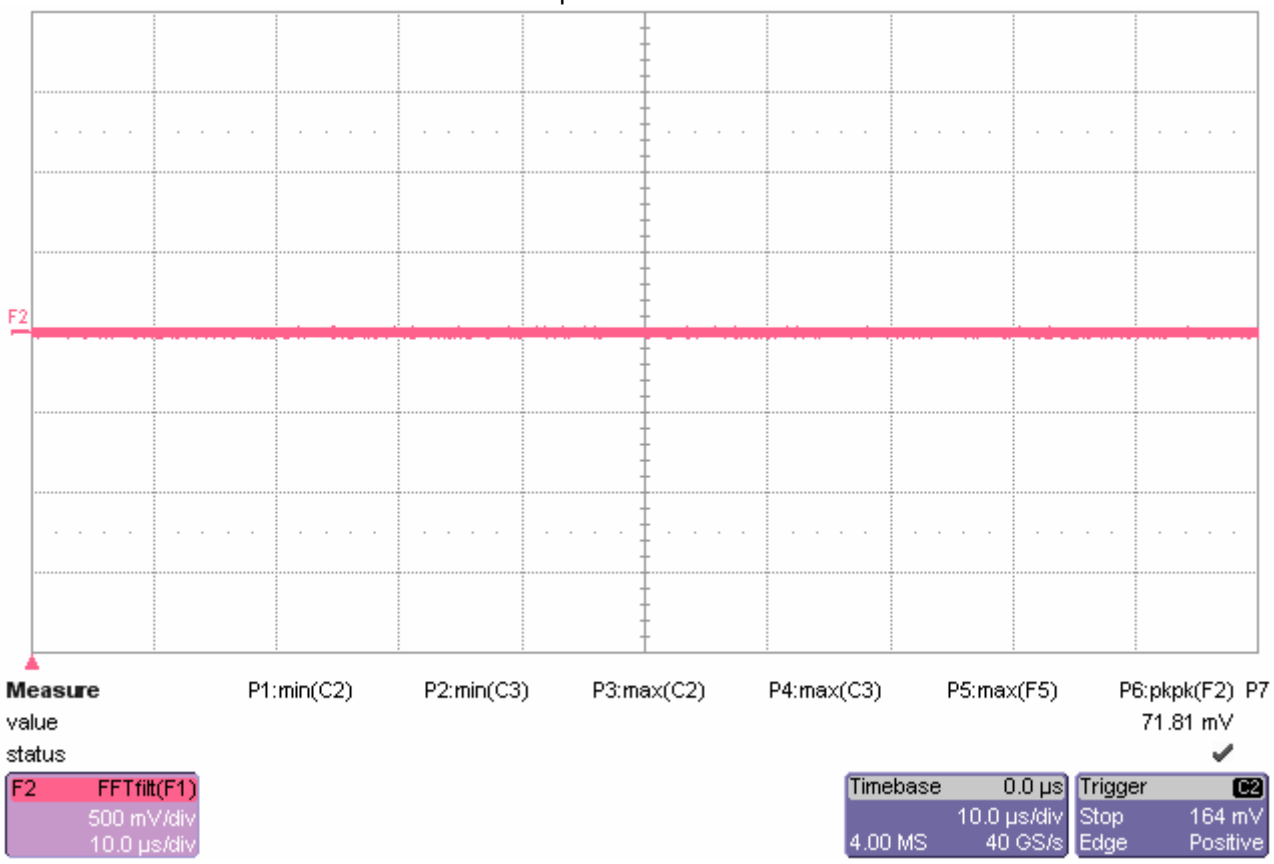
Pass

Limit Name: $V_{RX-CM-ACp-p}$
Current Value: 71.81 mV
Test Criteria: <= 270.00 mV

Timestamp: 2006/04/11 16:46:20

Figure 3.7 - RX AC Common Mode Voltage Pk-Pk

Timestamp: 2006/04/11 16:46:22



Test 3.2 - Maximum single-ended voltage in EI condition (AC + DC)

$V_{RX-IDLE-SE\_p}$

Maximum single-ended voltage in EI condition on Data+, DC + AC

Pass

Limit Name: $V_{RX-IDLE-SE}$
Current Value: 8.2 mV
Test Criteria: <= 75.0 mV
Timestamp: 2006/04/11 16:47:39

$V_{RX-IDLE-SE\_n}$

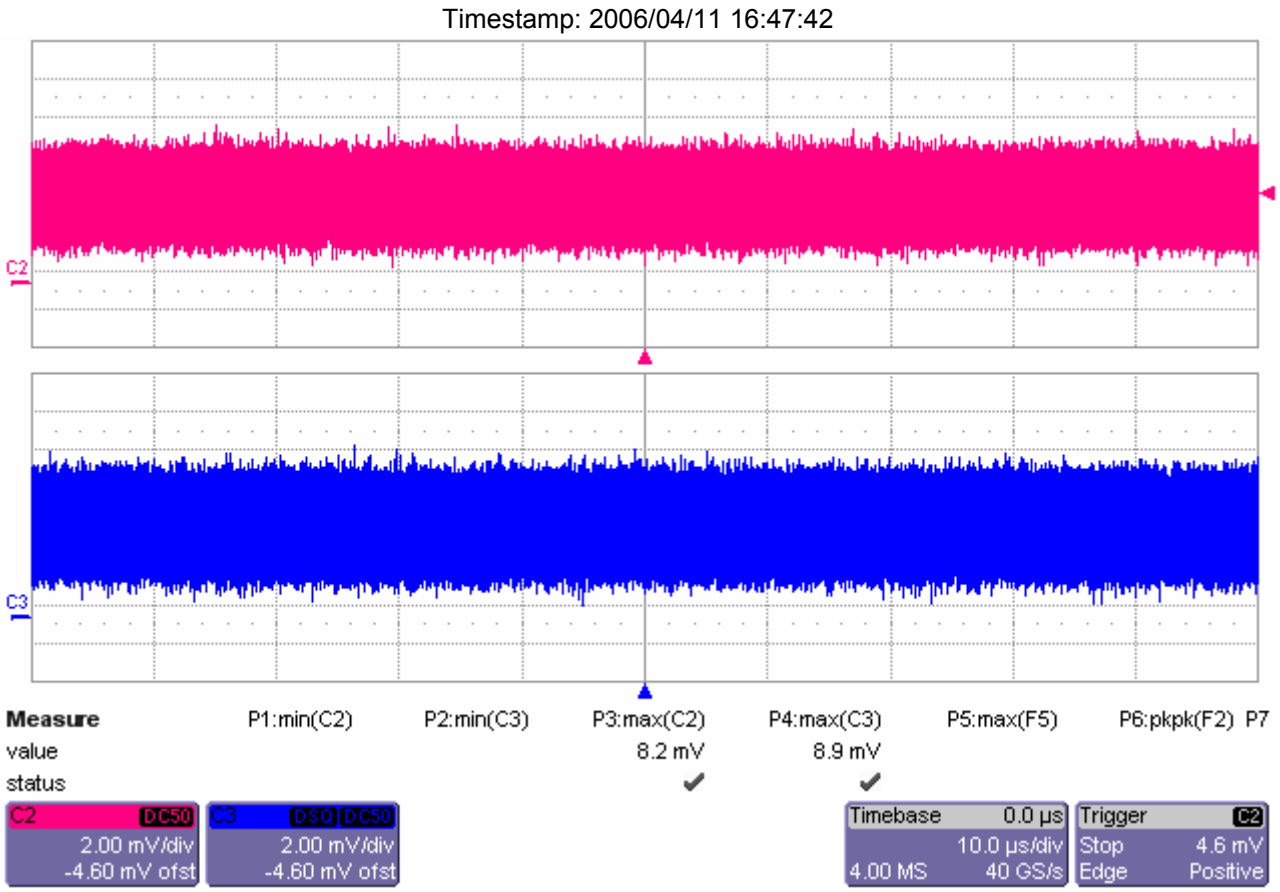
Maximum single-ended voltage in EI condition on Data-, DC + AC

Pass

Limit Name: $V_{RX-IDLE-SE}$
Current Value: 8.9 mV
Test Criteria: <= 75.0 mV

Timestamp: 2006/04/11 16:47:39

Figure 3.2 - RX Maximum Single-ended Voltage for EI Condition (AC + DC)



Test 1.2 - Single-ended maximum voltage

$V_{RefClk-max\_p}$

Single-ended maximum voltage on Refclk+

Pass

Limit Name: $V_{RefClk-max}$
Current Value: 812 mV
Test Criteria: <= 1.150 V
Timestamp: 2006/04/11 11:49:41

$V_{RefClk-max\_n}$

Single-ended maximum voltage on Refclk-

Pass

Limit Name: $V_{RefClk-max}$
Current Value: 825 mV

Test Criteria: <= 1.150 V
Timestamp: 2006/04/11 11:49:43

Test 1.3 - Single-ended minimum voltage

$V_{RefClk-min\_p}$

Single-ended minimum voltage on Refclk+

Pass

Limit Name: $V_{RefClk-min}$
Current Value: -20 mV
Test Criteria: >= -300 mV
Timestamp: 2006/04/11 11:49:43

$V_{RefClk-min\_n}$

Single-ended minimum voltage on Refclk-

Pass

Limit Name: $V_{RefClk-min}$
Current Value: -40 mV
Test Criteria: >= -300 mV
Timestamp: 2006/04/11 11:49:44

Test 1.4 - Absolute crossing point

$V_{RefClk-cross-min}$

Absolute Crossing Point - minimum

Pass

Limit Name: $V_{RefClk-cross-min}$
Current Value: 325.8 mV
Test Criteria: >= 250.0 mV
Timestamp: 2006/04/11 11:49:45

$V_{RefClk-cross-max}$

Absolute Crossing Point - maximum

Pass

Limit Name: $V_{RefClk-cross-max}$
Current Value: 370.8 mV
Test Criteria: <= 550.0 mV
Timestamp: 2006/04/11 11:49:46

Test 1.5 - VCross variation

$V_{RefClk\text{-}cross\text{-}delta}$

Vcross variation

Pass

Limit Name: $V_{RefClk\text{-}cross\text{-}delta}$
Current Value: 3.54340544786805E-02
Test Criteria: <=
Timestamp: 2006/04/11 11:49:47

Test 1.8 - % mismatch between rise and fall edge rates

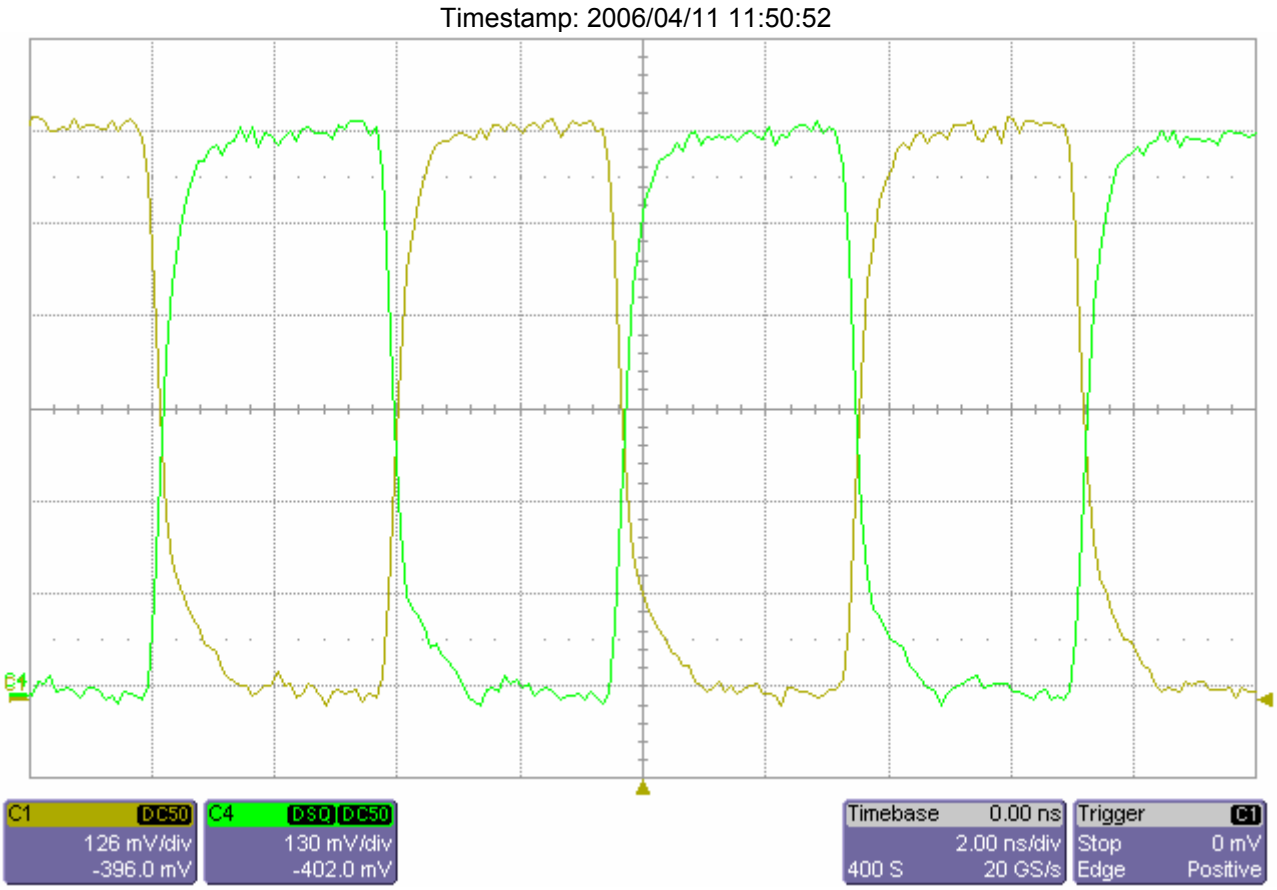
$ER_{RefClk\text{-}match}$

% mismatch between rise time on Refclk+ and fall time on Refclk-

Pass

Limit Name: $ER_{Refclk\text{-}Match}$
Current Value: 0.734923639691269
Test Criteria: <=
Timestamp: 2006/04/11 11:49:54

Figure 1.0 - Reference Clock Differential Single Lanes



Test 1.1 - Reference clock frequency

f_{RefClk}

Reference Clock Frequency

Pass

Limit Name: f_{Refclk}
Current Value: 133.032696 MHZ
Test Criteria: 190.00e6 < n < 200.10e6
Timestamp: 2006/04/11 11:51:14

Test 1.6 - Rising edge rate

$T_{RefClk-rise}$

Rising edge rate

Pass

Limit Name: $T_{Refclk-Rise}$
Current Value: 3.3029 GV/S
Test Criteria: 0.6e9 < n < 4.0e9
Timestamp: 2006/04/11 11:51:15

Test 1.7 - Falling edge rate

$T_{RefClk-fall}$

Falling edge rate

Pass

Limit Name: $T_{Refclk-Fall}$
Current Value: 3.0865 GV/S
Test Criteria: 0.6e9 < n < 4.0e9
Timestamp: 2006/04/11 11:51:15

Test 1.9 - Duty cycle of reference clock

$T_{RefClk-dutycycle}$

Duty Cycle of reference clock

Pass

Limit Name: $T_{Refclk-Dutycycle}$
Current Value: 49.56755 PCT
Test Criteria: 40 < n < 60
Timestamp: 2006/04/11 11:51:17

Test 1.10 - Reference clock jitter (rms), filtered

$T_{RefClk-jitter-rms}$

Reference clock jitter RMS filtered

Fail

Failure Explanation: cur [5.5026319405718E-12] is not <= ref [3.0e-12] (83.4211% error) keyword 0 numeric comparison failed
Limit Name: $T_{RefClk-jitter-rms}$
Current Value: 5.50 ps
Test Criteria: <= 2.50 ps
Timestamp: 2006/04/11 11:52:22

Figure 1.1 - Reference Clock Jitter Bathtub Curve

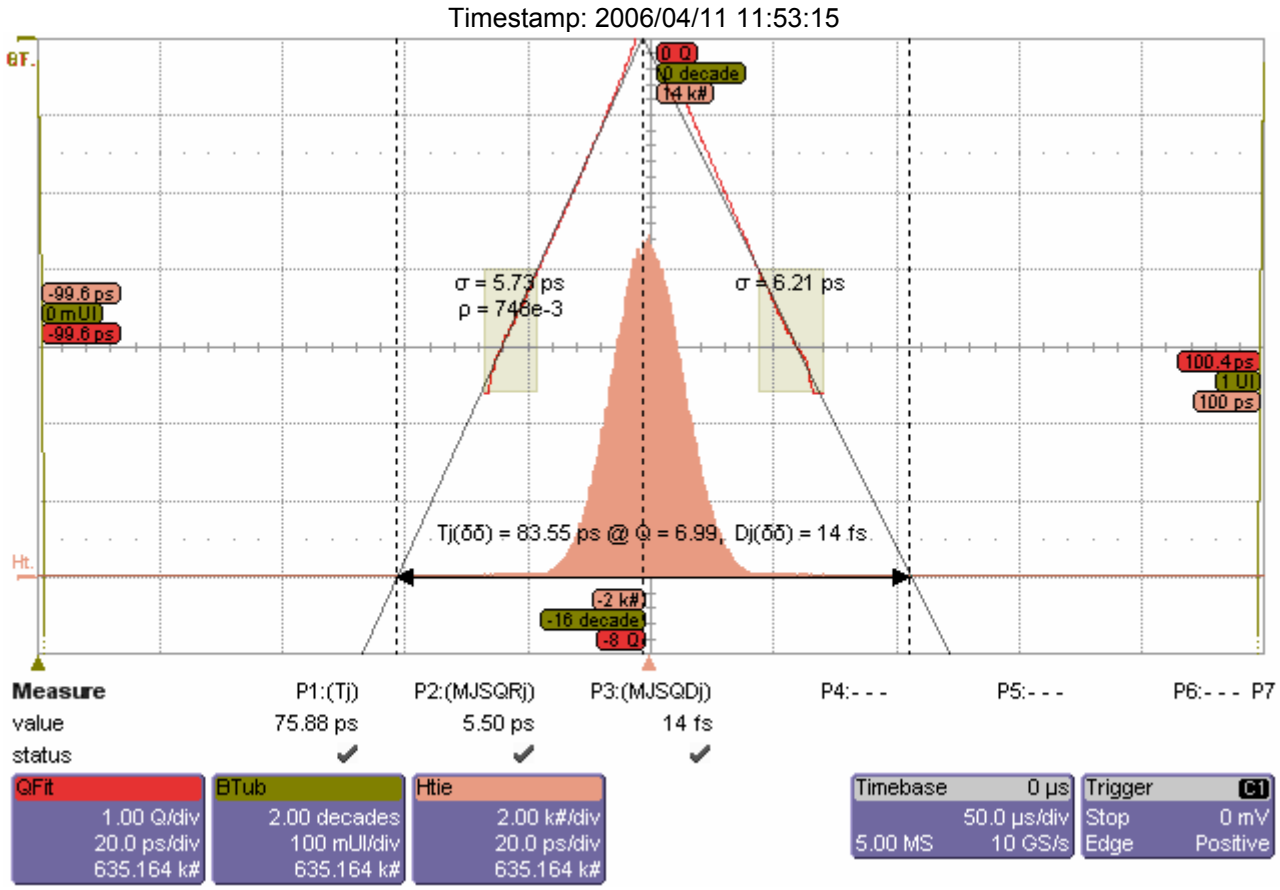
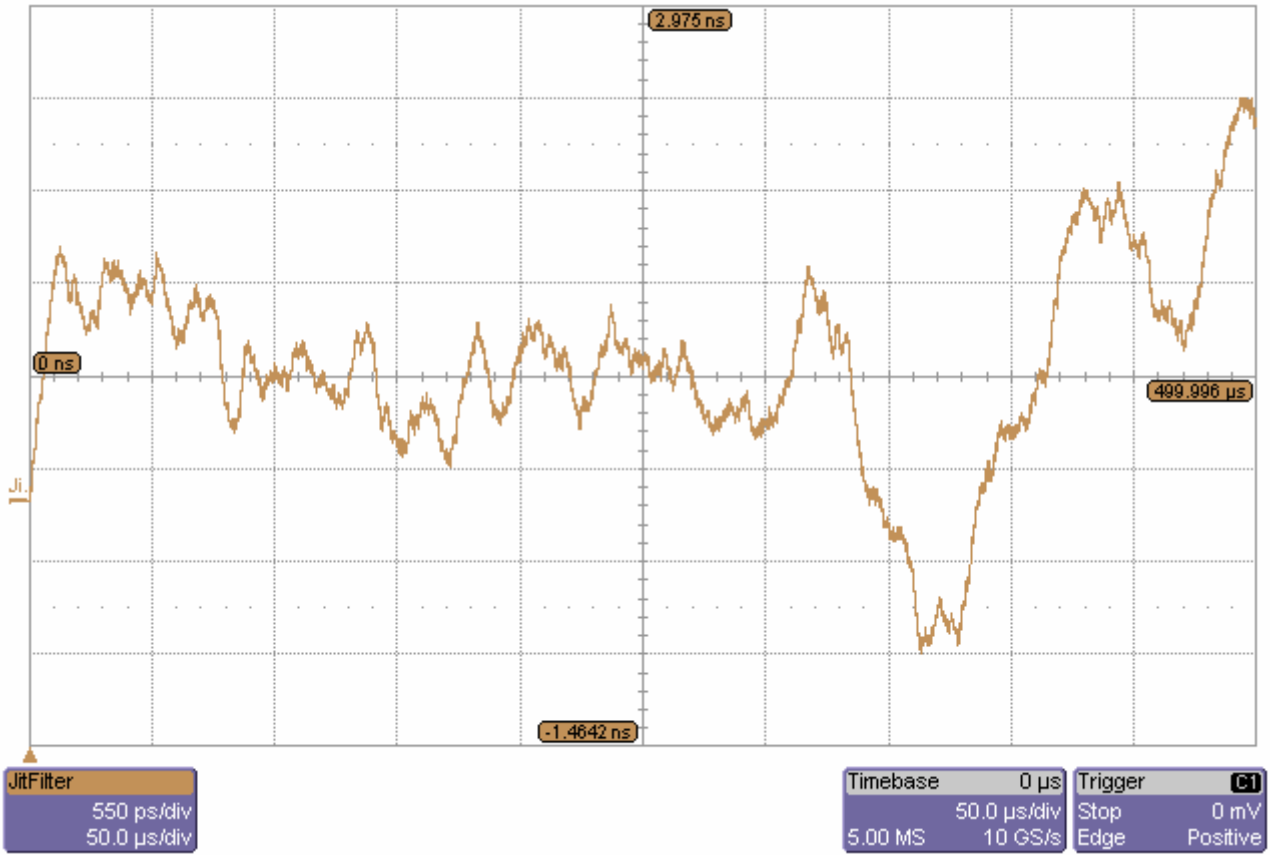


Figure 1.2 - Reference Clock SSC Track (PLL off)

Timestamp: 2006/04/11 11:54:10



Test 2.4 - DC common mode output voltage for large voltage swing

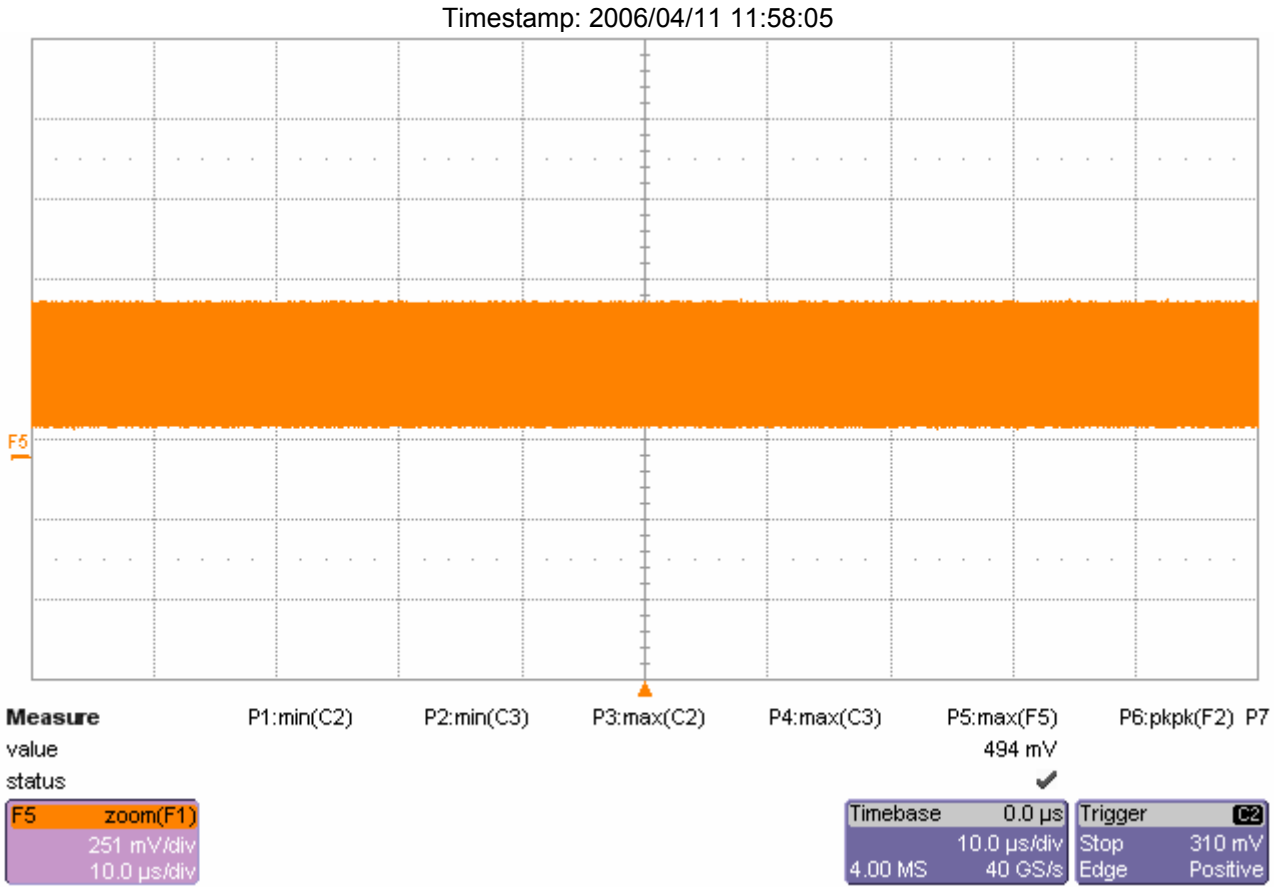
V_{TX-CM_L}

DC common mode output voltage for large voltage swing

Fail

Failure Explanation: cur [0.494304031133652] is not <= ref [375e-3] (31.8144% error) keyword 0 numeric comparison failed
Limit Name: V_{TX-CM_L}
Current Value: 494 mV
Test Criteria: <= 375 mV
Timestamp: 2006/04/11 11:57:19

Figure 2.4 - DC Common Mode for Large Voltage Swing.



Test 2.7 - AC peak-to-peak common mode output voltage for large voltage swing

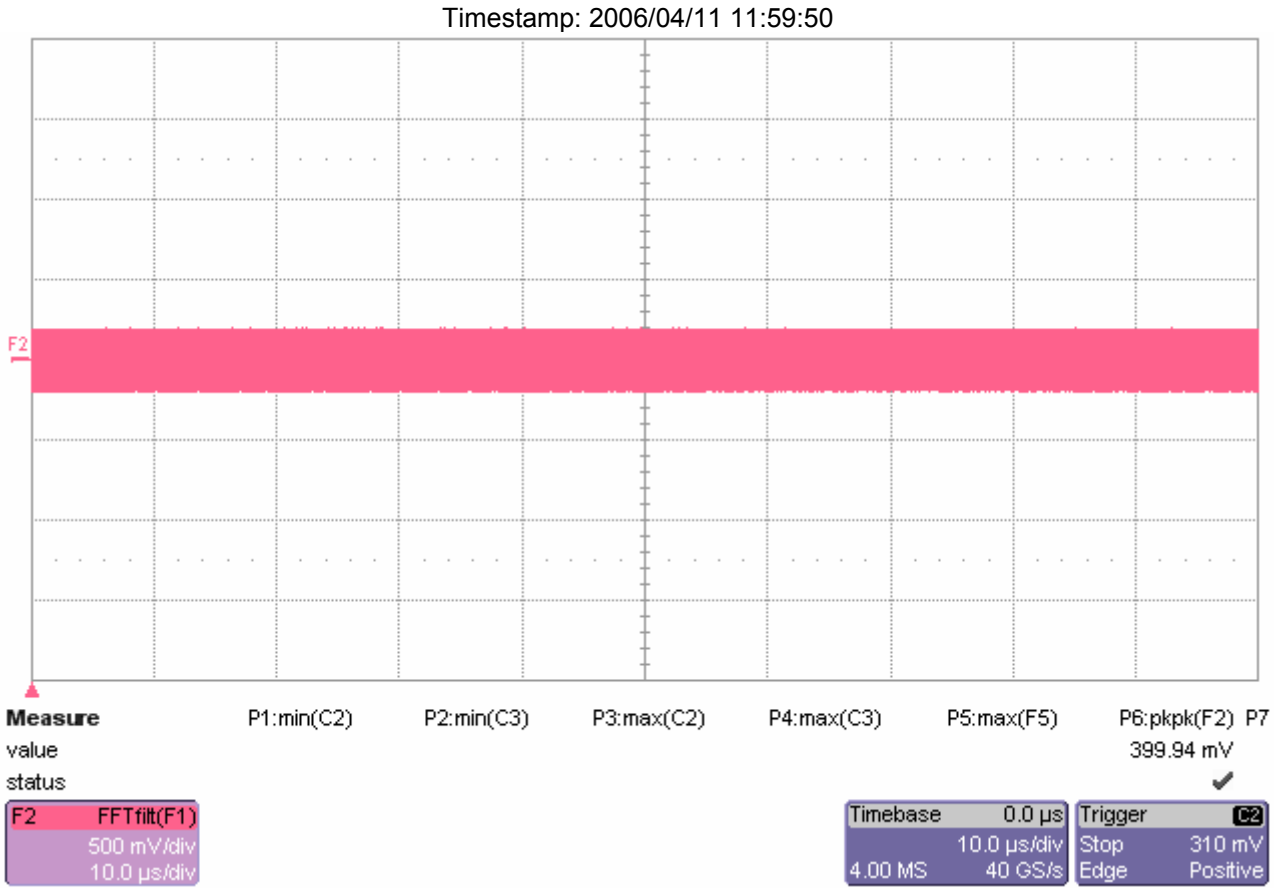
$V_{TX\text{-}CM\text{-}ACp\text{-}p\_L}$

AC peak-to-peak common mode output voltage for large voltage swing

Fail

Failure Explanation: cur [0.399938939102867] is not <= ref [90e-3] (344.377% error) keyword 0 numeric comparison failed
Limit Name: $V_{TX\text{-}CM\text{-}ACp\text{-}p\_L}$
Current Value: 399.94 mV
Test Criteria: <= 90.00 mV
Timestamp: 2006/04/11 11:58:53

Figure 2.7 - AC Common Mode for Large Voltage Swing.



Test 2.13 - Single-ended voltage on D+/D-

$V_{TX-SE-min\_p}$

Minimum Single-ended voltage on Data+

Pass

Limit Name: V_{TX-SE}
Current Value: 59 mV
Test Criteria: -75e-3 < n < 750e-3
Timestamp: 2006/04/11 12:00:03

$V_{TX-SE-min\_n}$

Minimum Single-ended voltage on Data-

Pass

Limit Name: V_{TX-SE}
Current Value: 43 mV
Test Criteria: -75e-3 < n < 750e-3
Timestamp: 2006/04/11 12:00:03

$V_{TX-SE-max\_p}$

Maximum Single-ended voltage on Data+

Pass

Limit Name: V_{TX-SE}
Current Value: 556 mV
Test Criteria: -75e-3 < n < 750e-3
Timestamp: 2006/04/11 12:00:04

$V_{TX-SE-max\_n}$

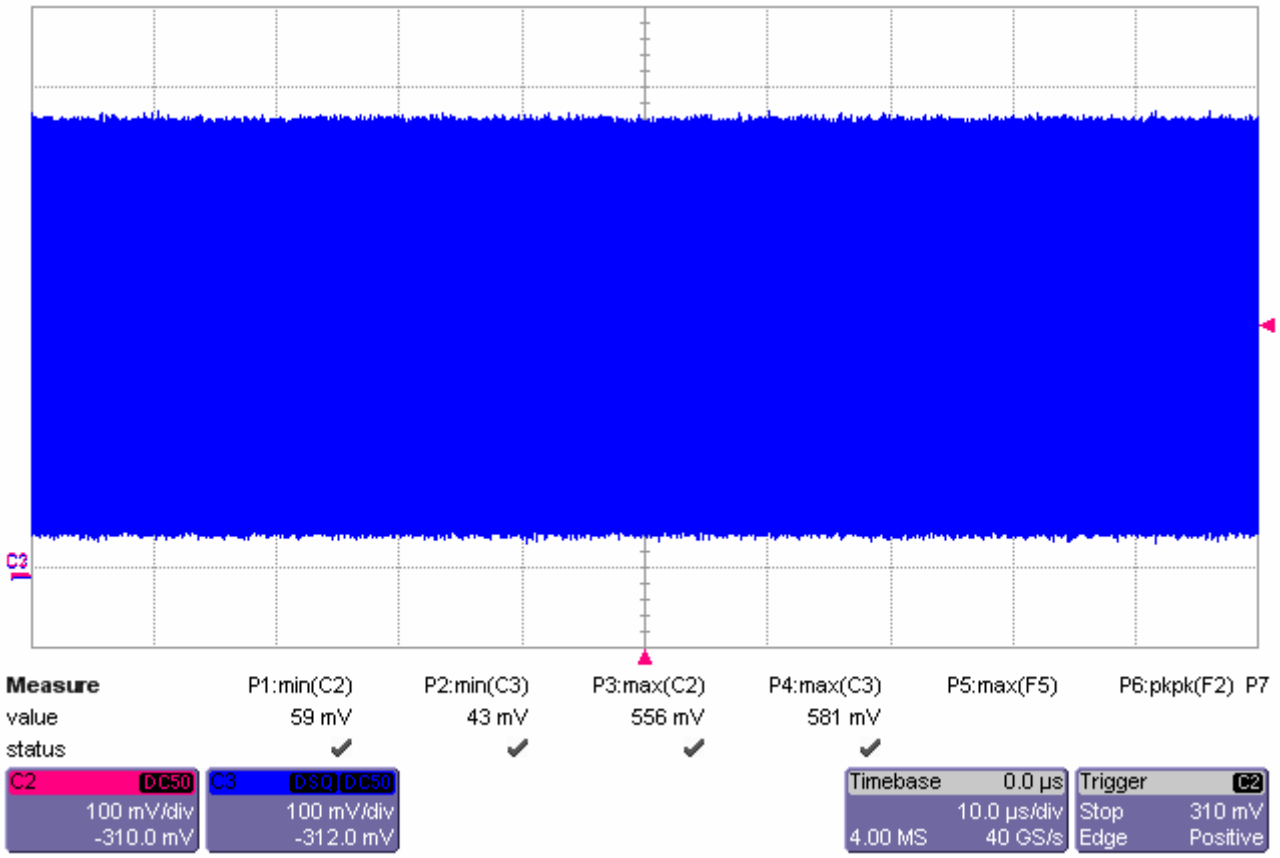
Maximum Single-ended voltage on Data-

Pass

Limit Name: V_{TX-SE}
Current Value: 581 mV
Test Criteria: -75e-3 < n < 750e-3
Timestamp: 2006/04/11 12:00:06

Figure 2.13 - Single-Ended Voltage

Timestamp: 2006/04/11 12:00:55



Test 2.8 - AC peak-to-peak common mode output voltage for regular voltage swing

$V_{TX-CM-ACp-p\_R}$

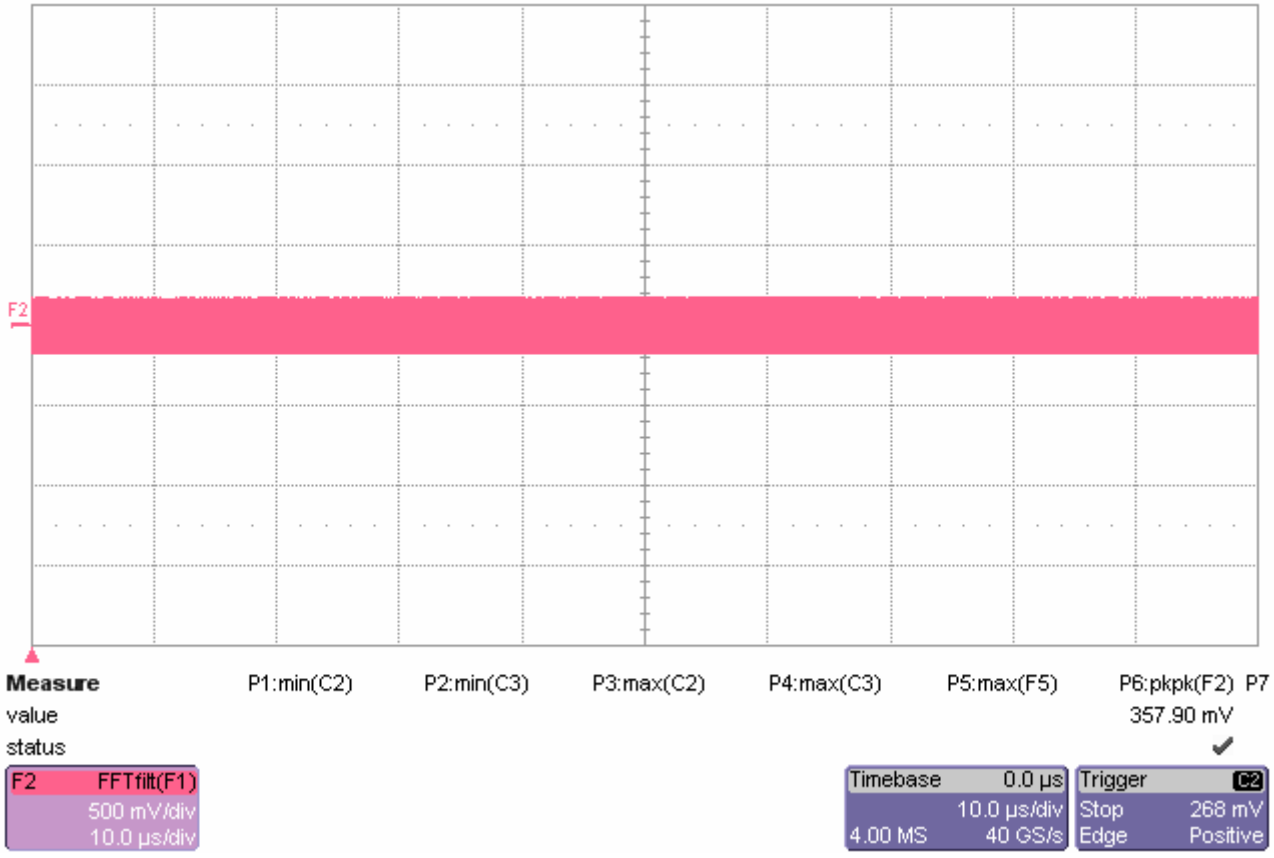
AC peak-to-peak common mode output voltage for regular voltage swing

Fail

Failure Explanation: cur [0.357904602926283] is not <= ref [80e-3] (347.381% error) keyword 0 numeric comparison failed
Limit Name: $V_{TX-CM-ACp-p\_R}$
Current Value: 357.90 mV
Test Criteria: <= 80.00 mV
Timestamp: 2006/04/11 12:02:38

Figure 2.8 - AC Common Mode for Regular Voltage Swing.

Timestamp: 2006/04/11 12:03:29



Test 2.5 - DC common mode output voltage for small voltage swing

V_{TX-CM_S}

DC common mode output voltage for small voltage swing

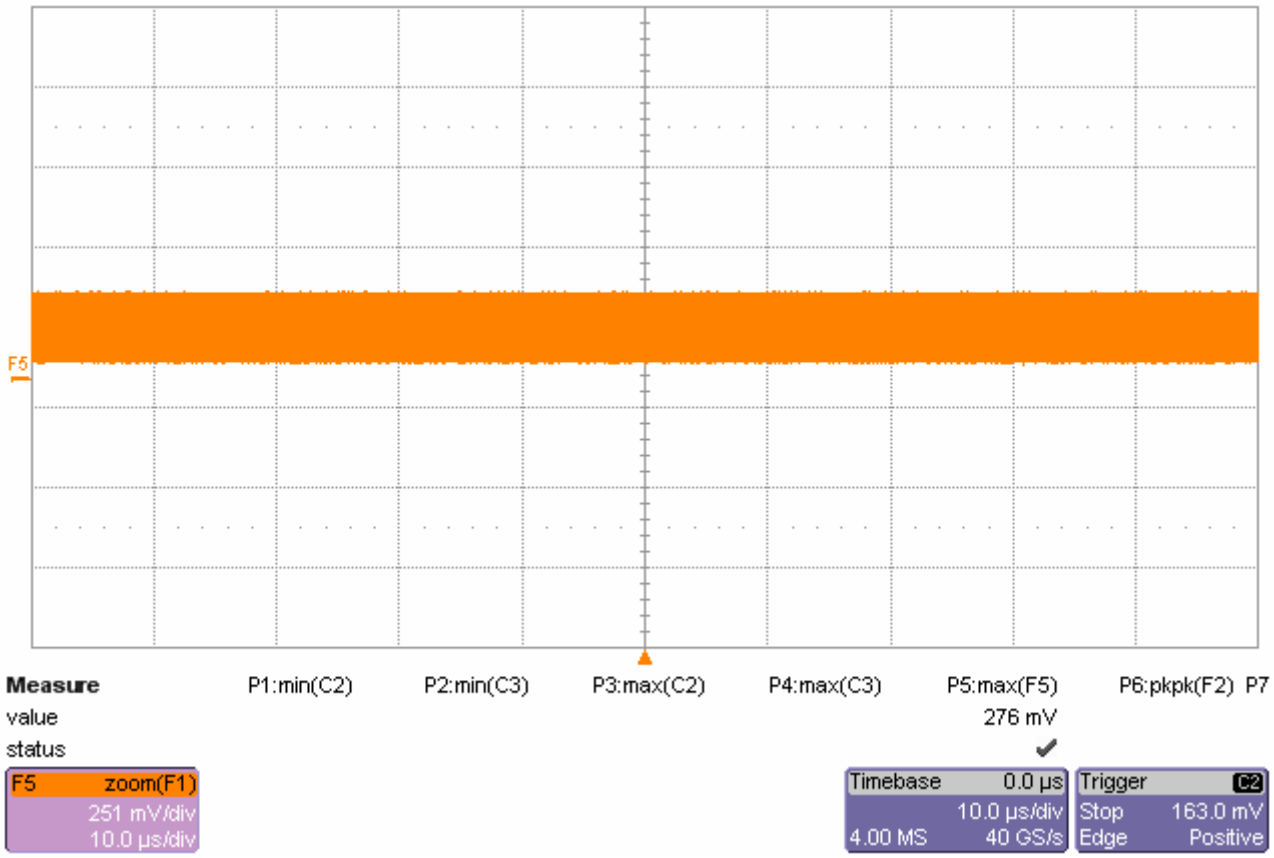
Pass

Limit Name: V_{TX-CM_S}
Current Value: 276 mV

Test Criteria: 135e-3 < n < 280e-3
Timestamp: 2006/04/11 12:04:47

Figure 2.4 - DC Common Mode for Large Voltage Swing.

Timestamp: 2006/04/11 12:06:04



Test 2.9 - AC peak-to-peak common mode output voltage for small voltage swing

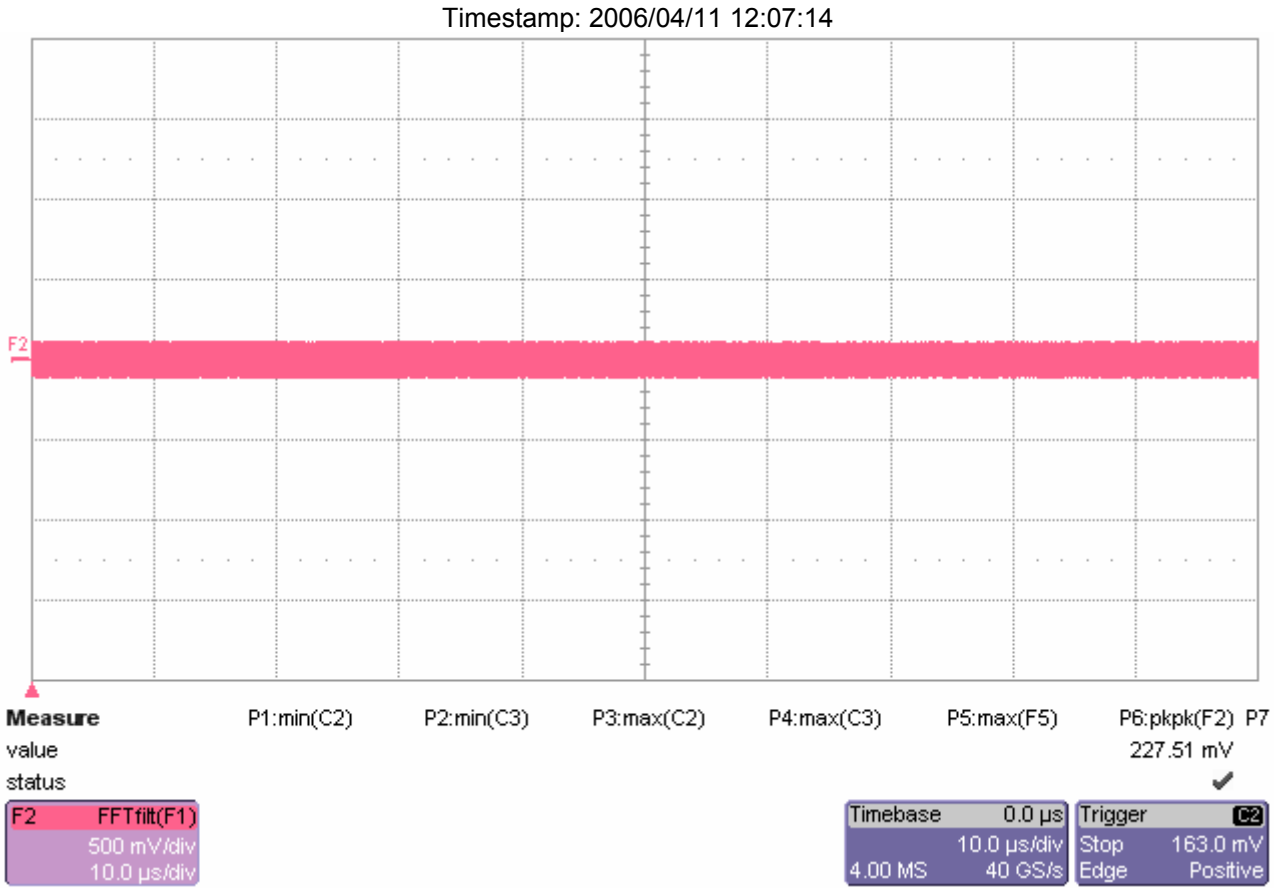
$V_{TX\text{-}CM\text{-}ACp\text{-}p\_S}$

AC peak-to-peak common mode output voltage for small voltage swing

Fail

Failure Explanation: cur [0.227512322388066] is not <= ref [70e-3] (225.018% error) keyword 0 numeric comparison failed
Limit Name: $V_{TX\text{-}CM\text{-}ACp\text{-}p\_S}$
Current Value: 227.51 mV
Test Criteria: <= 70.00 mV
Timestamp: 2006/04/11 12:06:35

Figure 2.9 - AC Common Mode for Small Voltage Swing.



Test 2.10 - Maximum single-ended voltage in EI condition, DC + AC

$V_{TX-IDLE-SE\_p}$

Maximum single-ended voltage in EI condition, DC + AC on Data+

Pass

Limit Name: $V_{TX-IDLE-SE}$
Current Value: 6.4 mV
Test Criteria: <= 50.0 mV
Timestamp: 2006/04/11 12:08:30

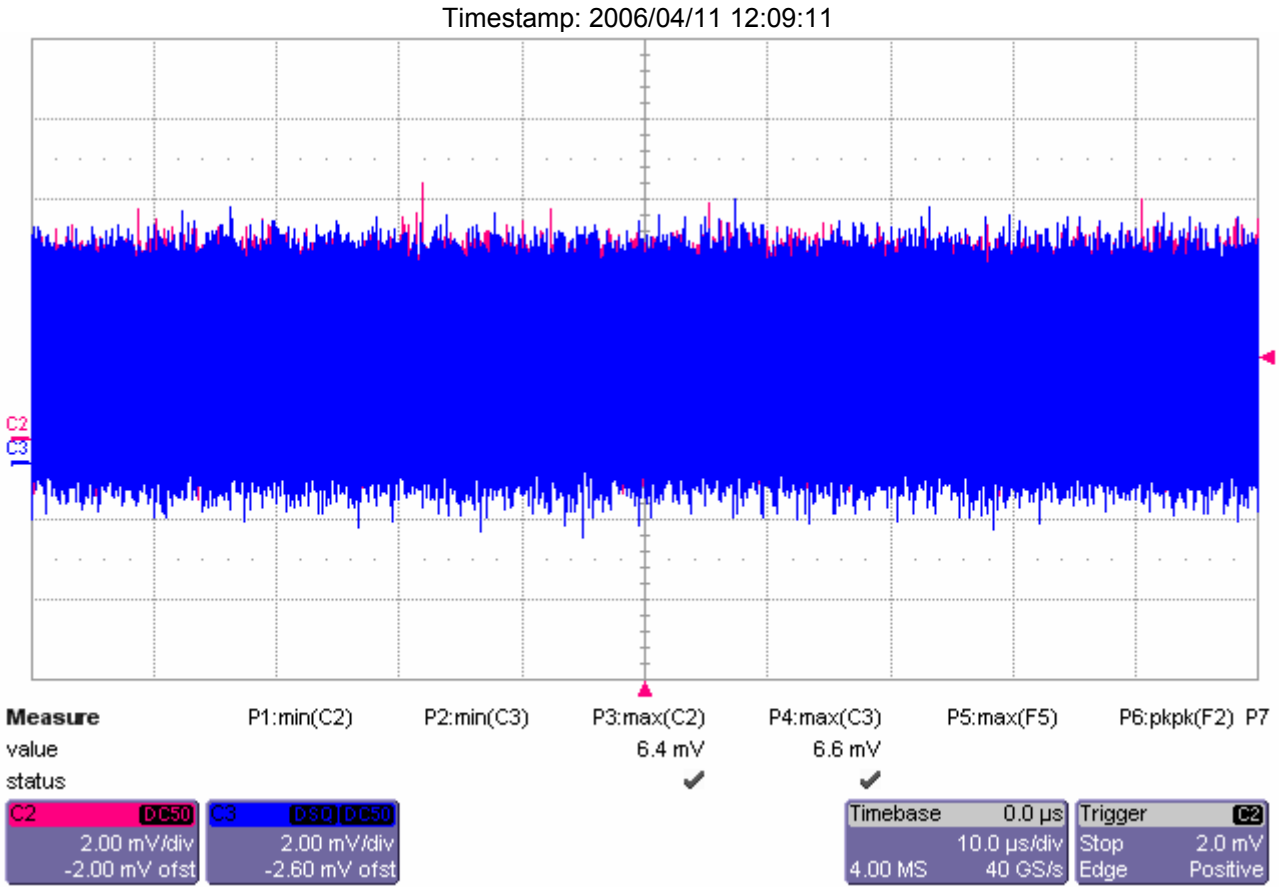
$V_{TX-IDLE-SE\_n}$

Maximum single-ended voltage in EI condition, DC + AC on Data-

Pass

Limit Name: $V_{TX-IDLE-SE}$
Current Value: 6.6 mV
Test Criteria: <= 50.0 mV
Timestamp: 2006/04/11 12:08:31

Figure 2.11 - Maximum Single-ended Voltage in EI Condition (DC only)



Test 2.11 - Maximum single-ended voltage in EI condition, DC only

$V_{TX-IDLE-SE-DC\_p}$

Maximum single-ended voltage in EI condition, DC only on Data+

Pass

Limit Name: $V_{TX-IDLE-SE-DC}$
Current Value: 6.4 mV
Test Criteria: <= 20.0 mV
Timestamp: 2006/04/11 12:09:21

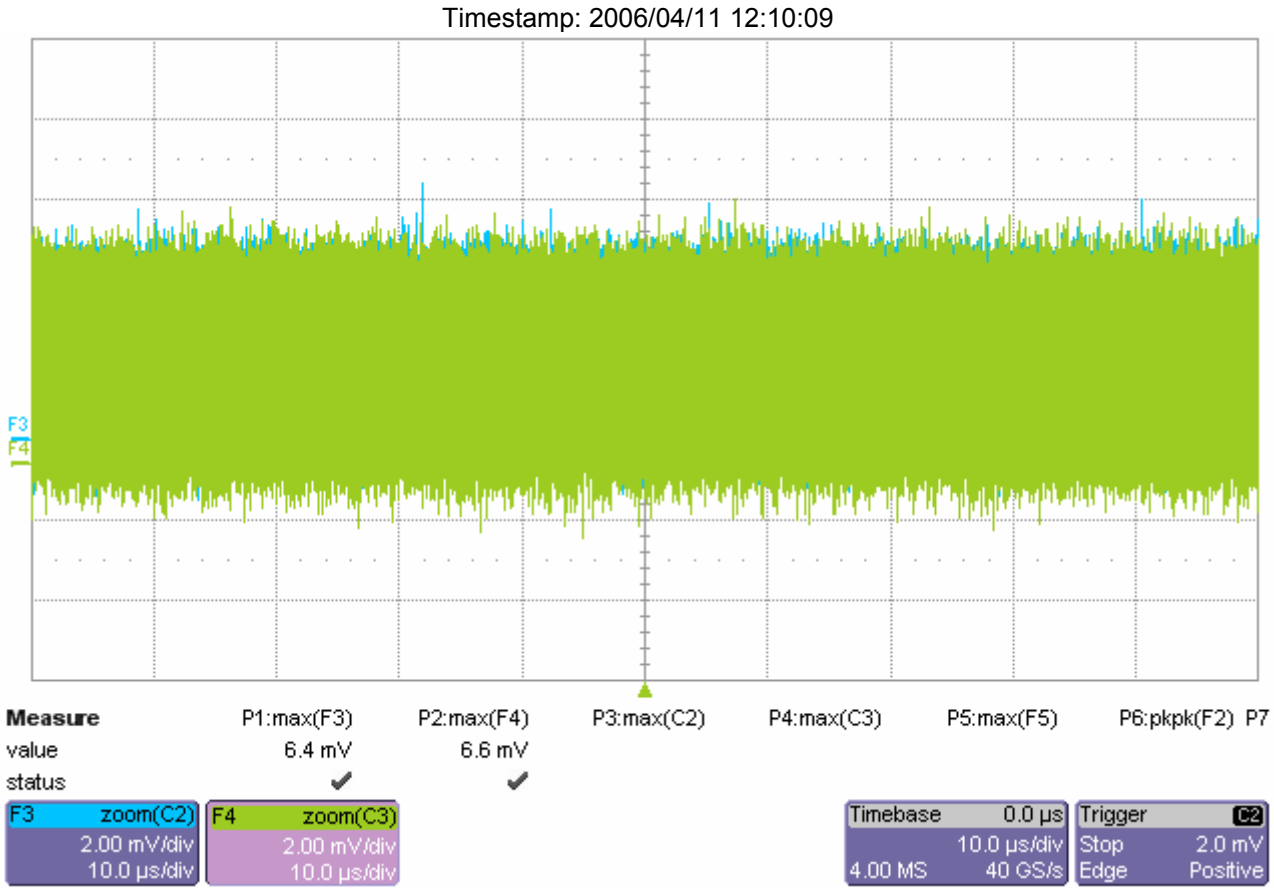
$V_{TX-IDLE-SE-DC\_n}$

Maximum single-ended voltage in EI condition, DC only on Data-

Pass

Limit Name: $V_{TX-IDLE-SE-DC}$
Current Value: 6.6 mV
Test Criteria: <= 20.0 mV
Timestamp: 2006/04/11 12:09:22

Figure 2.10 - Maximum Single-ended Voltage in EI Condition (AC + DC)



Test 2.1 - Differential peak-to-peak output voltage for large voltage swing

$V_{TX-DIFFp-p\_L-min}$

Differential peak-to-peak output voltage for large voltage swing - minimum

Fail

Failure Explanation: cur [0.777033396457085] is not >= ref [900e-3] (13.663% error) keyword 0 numeric comparison failed
Limit Name: $V_{TX-DIFFp-p\_L-min}$
Current Value: 777 mV
Test Criteria: >= 900 mV
Timestamp: 2006/04/11 12:13:06

$V_{TX-DIFFp-p\_L-max}$

Differential peak-to-peak output voltage for large voltage swing - maximum

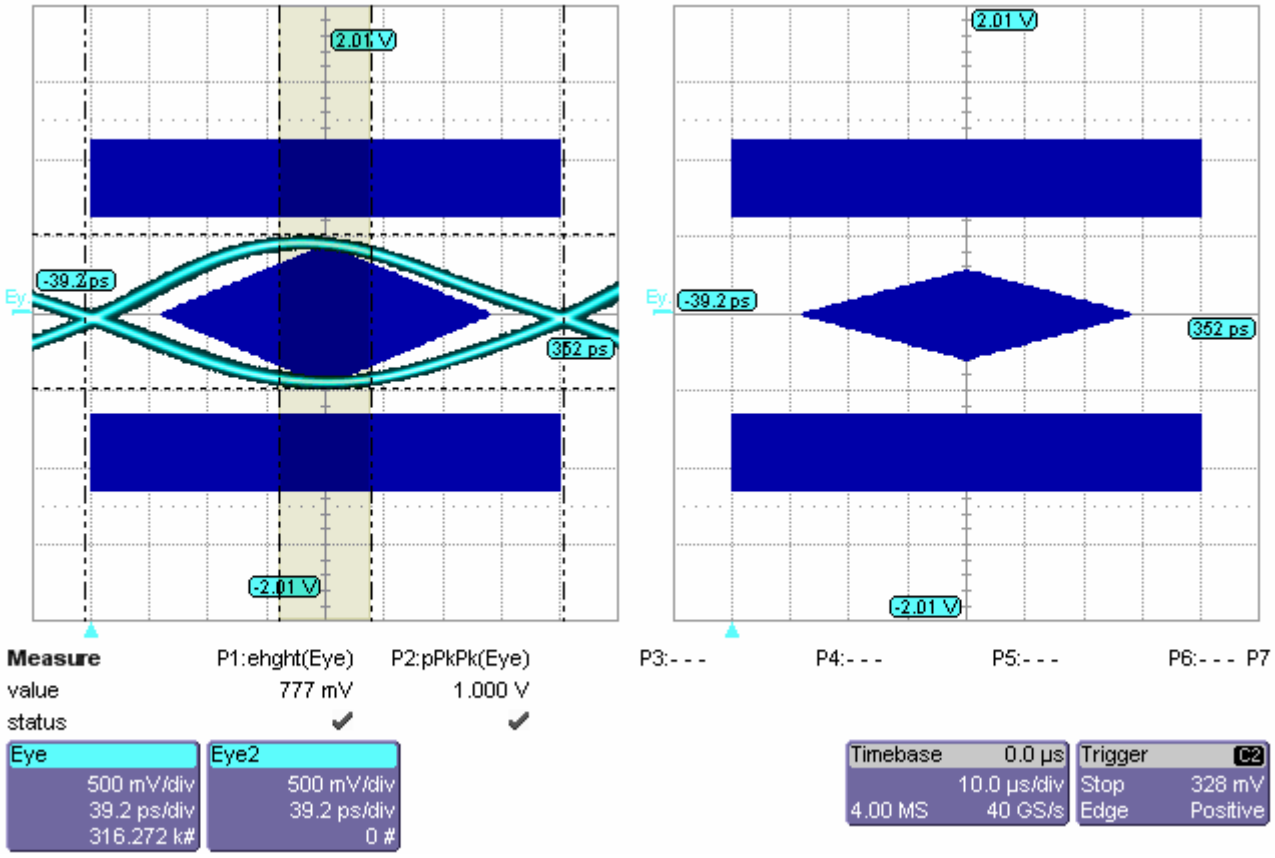
Pass

Limit Name: $V_{TX-DIFFp-p\_L-max}$
Current Value: 1.000 V
Test Criteria: <= 1.300 V

Timestamp: 2006/04/11 12:13:06

Figure 2.1 - Differential Pk-Pk Output Voltage for Large Voltage Swing.

Timestamp: 2006/04/11 12:13:42



Test 2.2 - Differential peak-to-peak output voltage for regular voltage swing

$V_{TX-DIFFp-p\_R-min}$

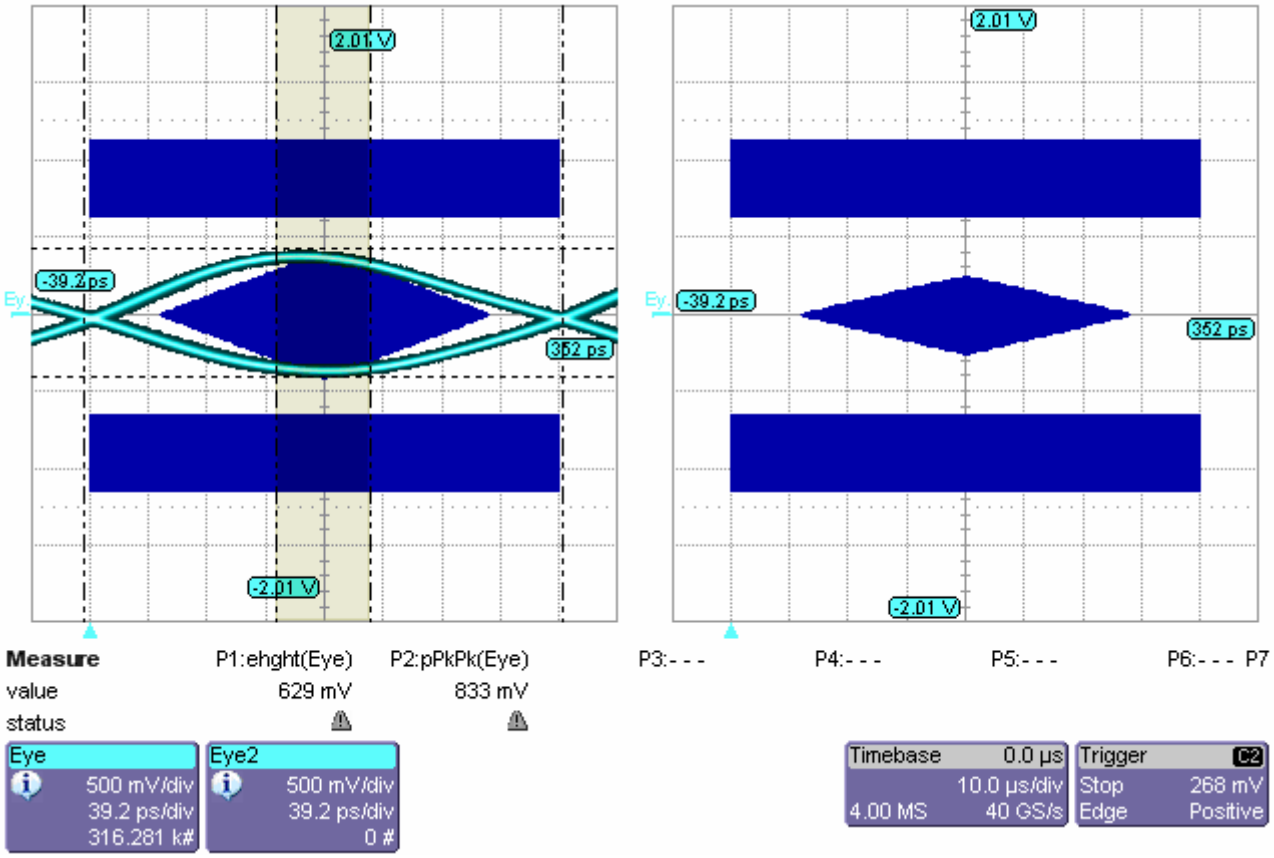
Differential peak-to-peak output voltage for regular voltage swing - minimum

Fail

Failure Explanation: cur [0.629425207628469] is not >= ref [800e-3] (21.3218% error) keyword 0 numeric comparison failed
Limit Name: $V_{TX-DIFFp-p\_R-min}$
Current Value: 629 mV
Test Criteria: >= 800 mV
Timestamp: 2006/04/11 12:15:10

Figure 2.2 - Differential Pk-Pk Output Voltage for Regular Voltage Swing.

Timestamp: 2006/04/11 12:15:44



Test 2.3 - Differential peak-to-peak output voltage for regular small swing

$V_{TX\text{-}DIFFp\text{-}p\_S\text{-}min}$

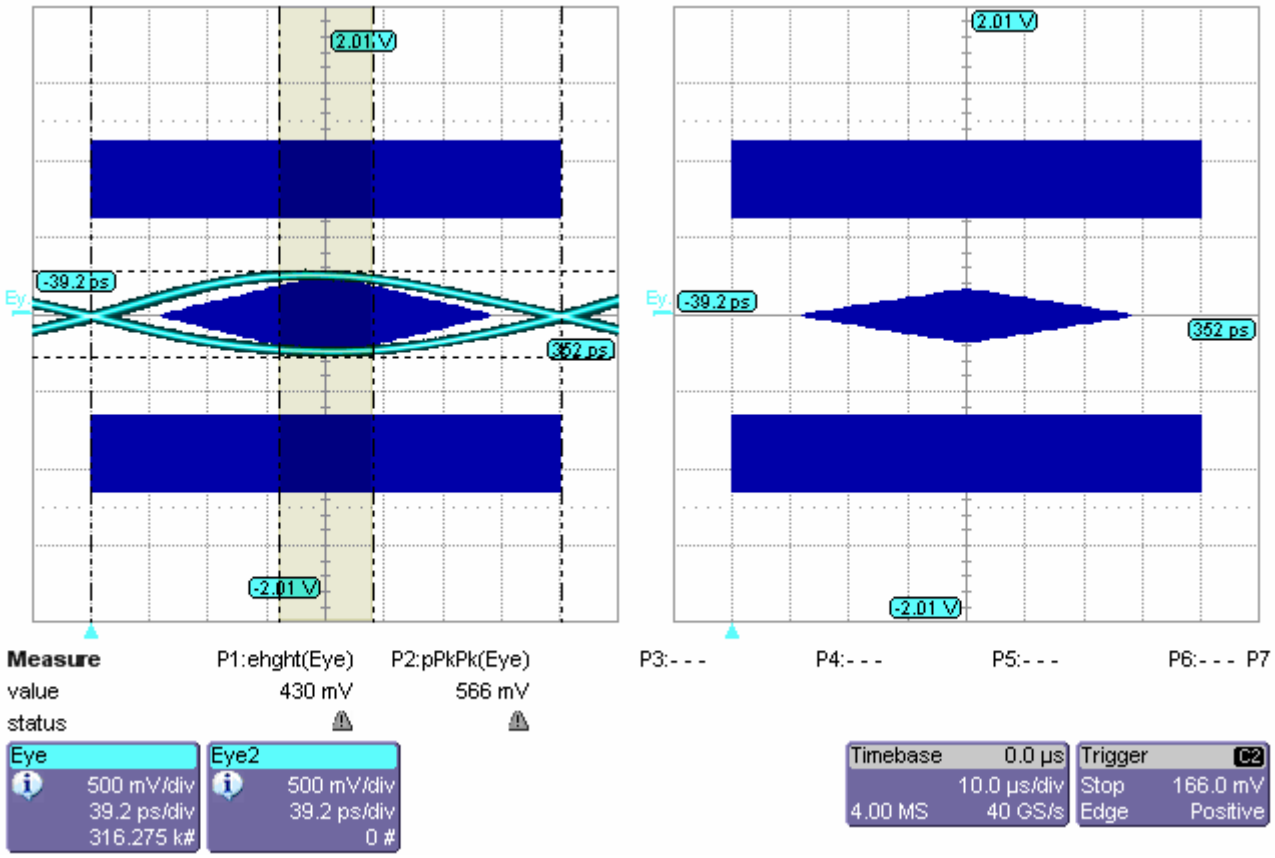
Differential peak-to-peak output voltage for regular small swing - minimum

Fail

Failure Explanation: cur [0.429533758721019] is not >= ref [520e-3] (17.3974% error) keyword 0 numeric comparison failed
Limit Name: $V_{TX\text{-}DIFFp\text{-}p\_S\text{-}min}$
Current Value: 430 mV
Test Criteria: >= 520 mV
Timestamp: 2006/04/11 12:17:19

Figure 2.3 - Differential Pk-Pk Output Voltage for Small Voltage Swing.

Timestamp: 2006/04/11 12:17:52



Test 2.14 - Minimum TX eye width

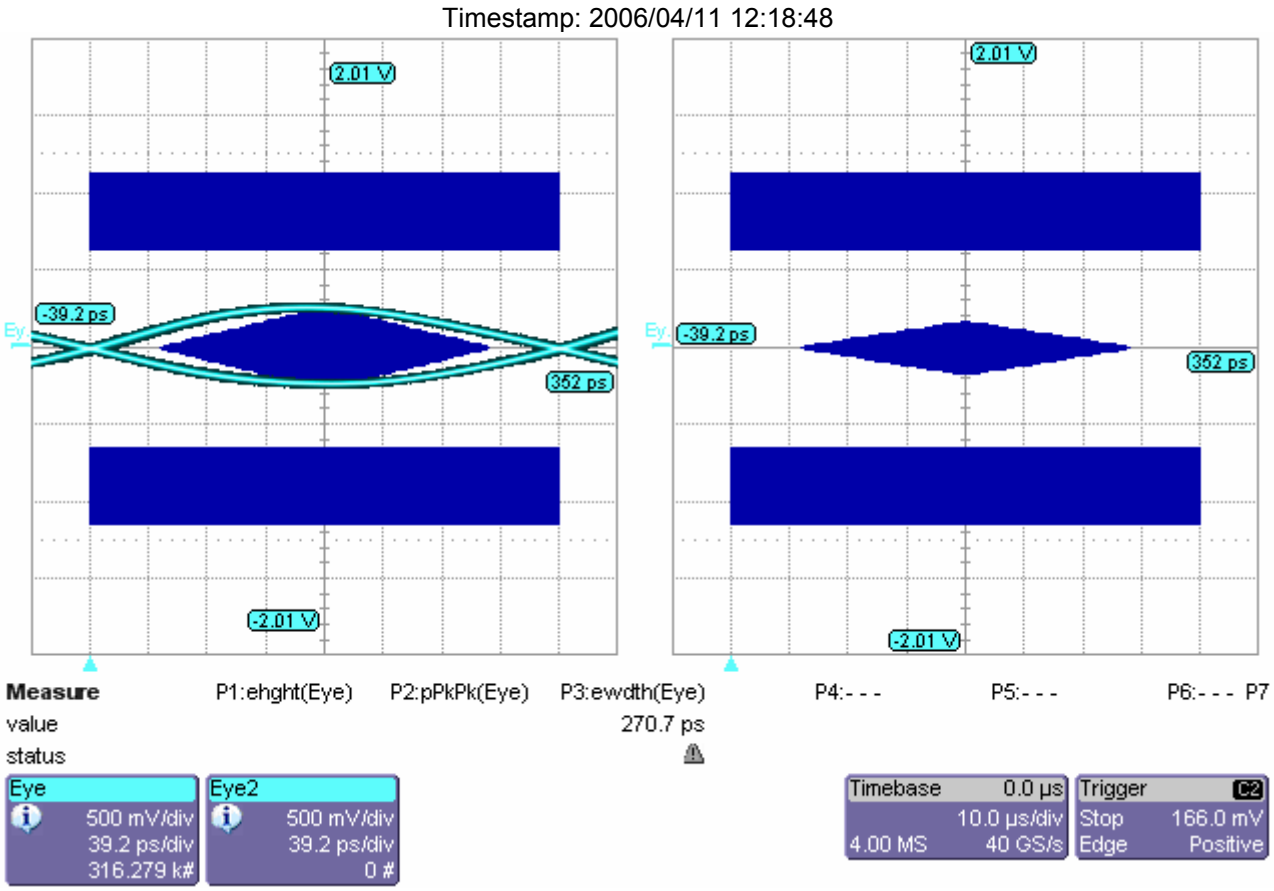
$T_{TX\text{-}eye\text{-}min}$

Minimum TX Eye Width

Pass

Limit Name: $T_{TX\text{-}EYE\text{-}MIN}$
Current Value: 0.866121578401112
Test Criteria: >=
Timestamp: 2006/04/11 12:18:11

Figure 2.14 - Maximum TX Eye Width



Test 2.17 - Differential TX output rise time

$T_{TX\text{-}rise}$

Differential TX output Rise

Fail

Failure Explanation: Current value 1.16706e-010 outside the Limit TTX-RISE Lower limit: 3e-011, Upper limit: 9e-011 Within limit test failed
Limit Name: $T_{TX\text{-}RISE}$
Current Value: 116.706 ps
Test Criteria: 30e-12 < n < 90e-12
Timestamp: 2006/04/11 12:19:24

Test 2.18 - Differential TX output fall time

$T_{TX\text{-}fall}$

Differential TX output Fall

Fail

Failure Explanation: Current value 1.33471e-010 outside the Limit TTX-FALL Lower limit: 3e-011, Upper limit: 9e-011 Within limit test failed
Limit Name: $T_{TX\text{-}FALL}$

Current Value: 133.471 ps
Test Criteria: 30e-12 < n < 90e-12
Timestamp: 2006/04/11 12:19:30

Test 2.19 - Mismatch between rise and fall times

$T_{TX\text{-}RF\text{-}mismatch}$

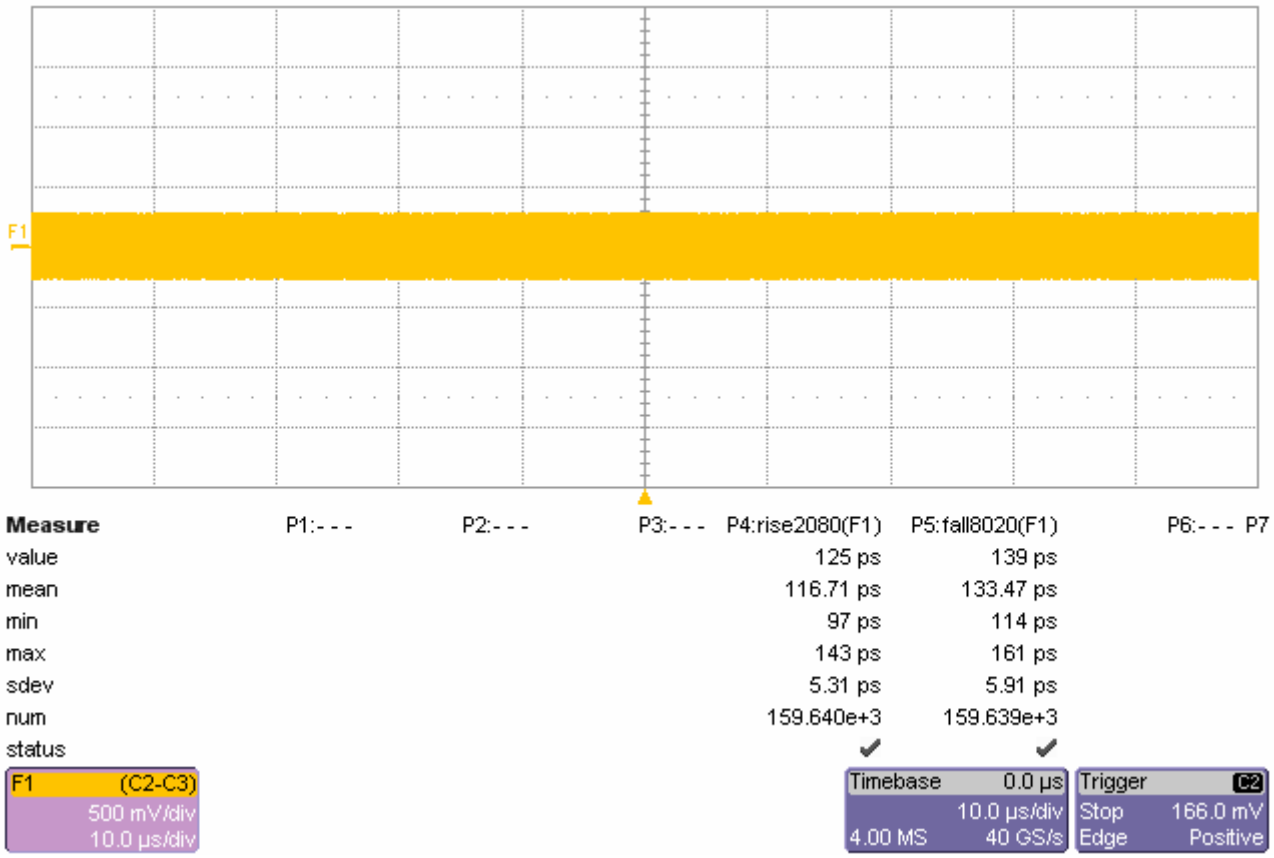
Mismatch between rise and fall times

Pass

Limit Name: $T_{TX\text{-}RF\text{-}MISMATCH}$
Current Value: 1.67649761846815E-11
Test Criteria: <=
Timestamp: 2006/04/11 12:19:31

Figure 2.17 - Rise and Fall Time Measurements.

Timestamp: 2006/04/11 12:19:58



Test 2.6.1 - De-emphasized differential output voltage ratio for -3.5 dB de-emphasis

$V_{TX-DE-3.5-ratio}$

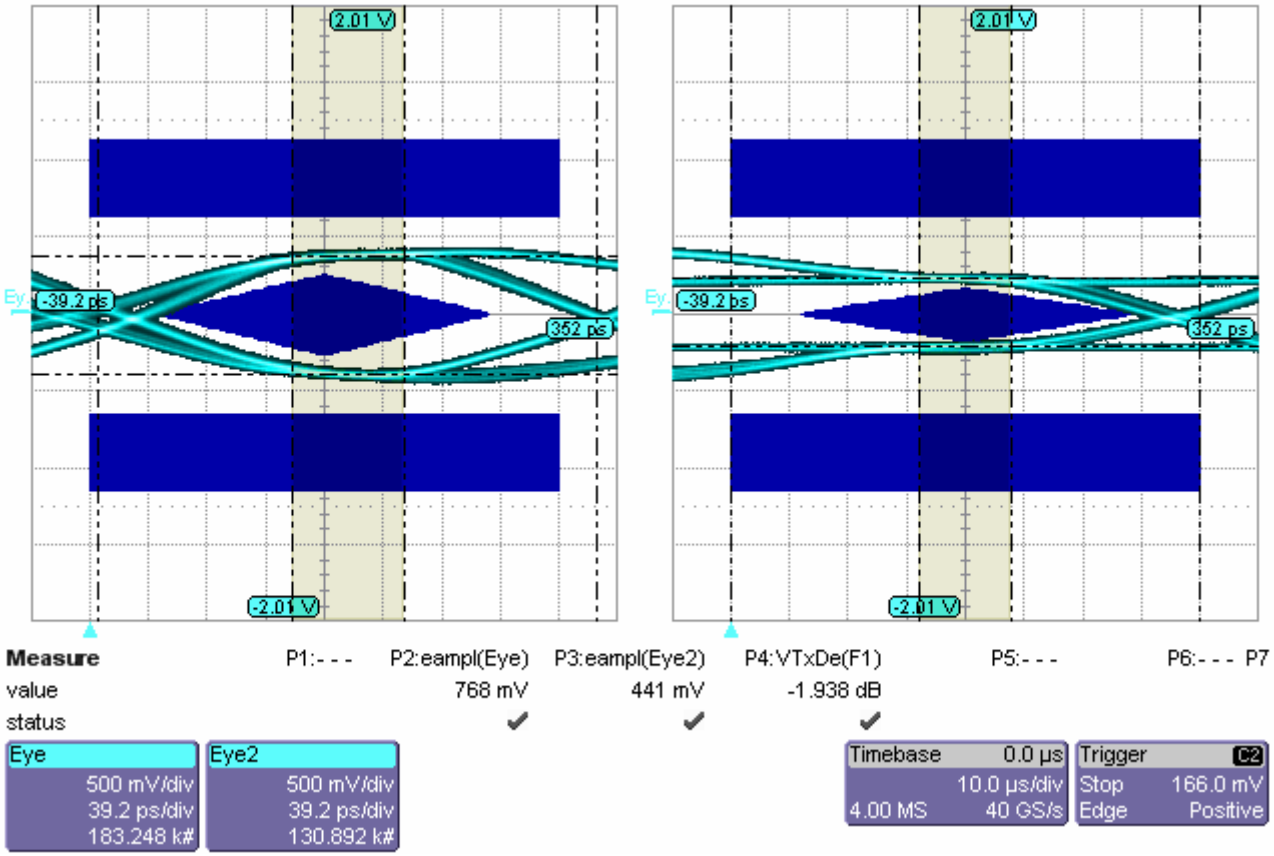
De-emphasized differential output voltage ratio for -3.5dB de-emphasis

Fail

Failure Explanation: Current value -4.82754 outside the Limit VTX-DE-3.5-Ratio Lower limit: -3, Upper limit: -4 Within limit test failed
Limit Name: $V_{TX-DE-3.5-Ratio}$
Current Value: -4.82753882732286
Test Criteria: -3 < n < -4
Timestamp: 2006/04/11 12:26:20

Figure 2.6.1 - TX De-emphasis -3.5 dB Ratio

Timestamp: 2006/04/11 12:26:45



Test 2.6.2 - De-emphasized differential output voltage ratio for -6 dB de-emphasis

$V_{TX-DE-6-ratio}$

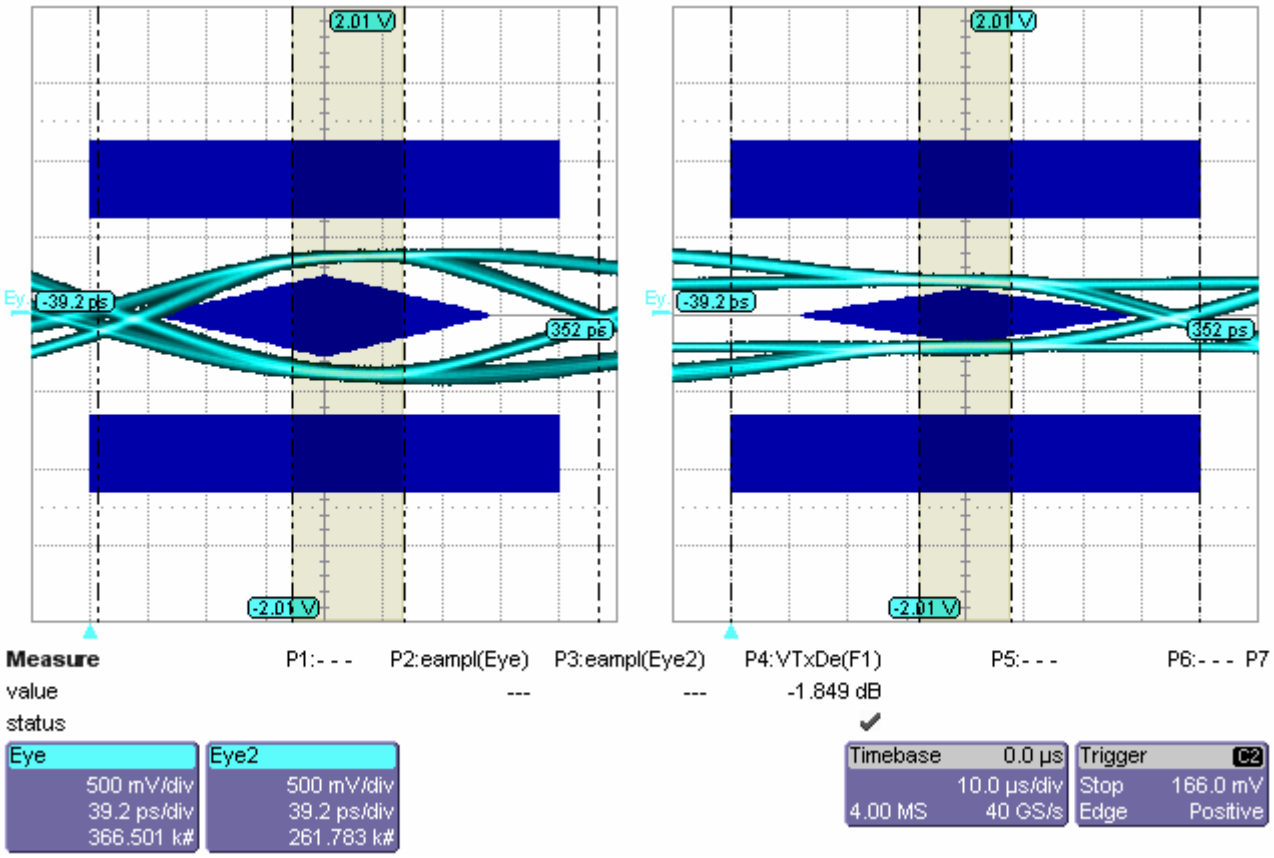
De-emphasized differential output voltage ratio for -6dB de-emphasis

Fail

Failure Explanation: keyword 0 numeric comparison failed either the current value, or the reference value is not numeric. cur [No Data Available] != ref [0.541368317928483]
Limit Name: $V_{TX-DE-6.0-Ratio}$
Current Value: No Data Available
Test Criteria: -5 < n < -7
Timestamp: 2006/04/11 12:27:49

Figure 2.6.2 - TX De-emphasis -6 dB Ratio

Timestamp: 2006/04/11 12:28:30



Test 2.16 - Instantaneous pulse width

$T_{TX-pulse}$

Minimum pulse width

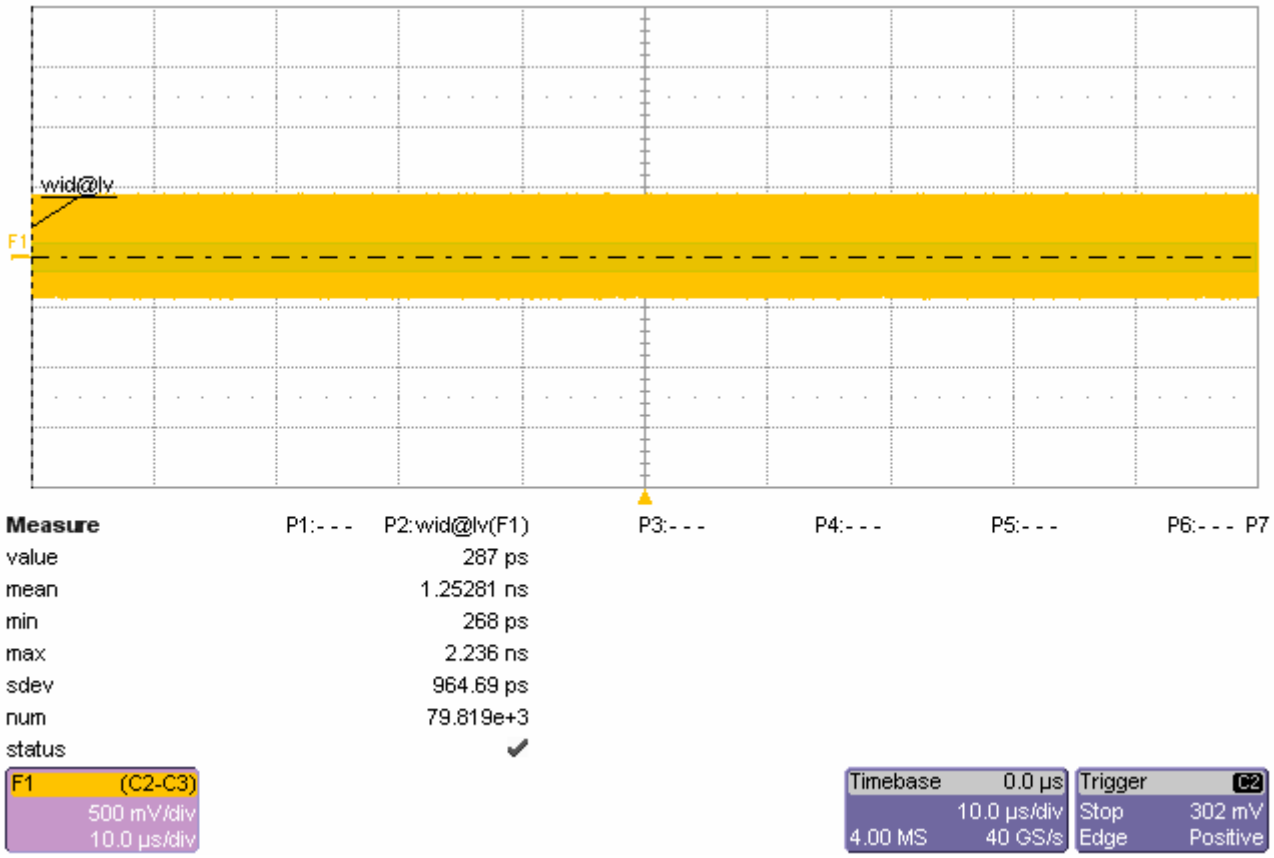
Pass

Limit Name: $T_{TX-PULSE}$
Current Value: 0.858743838018372

Test Criteria: >=
Timestamp: 2006/04/11 12:31:58

Figure 2.16 - TX Instantaneous Pulse Width

Timestamp: 2006/04/11 12:32:37



Test 2.15 - Maximum TX deterministic jitter

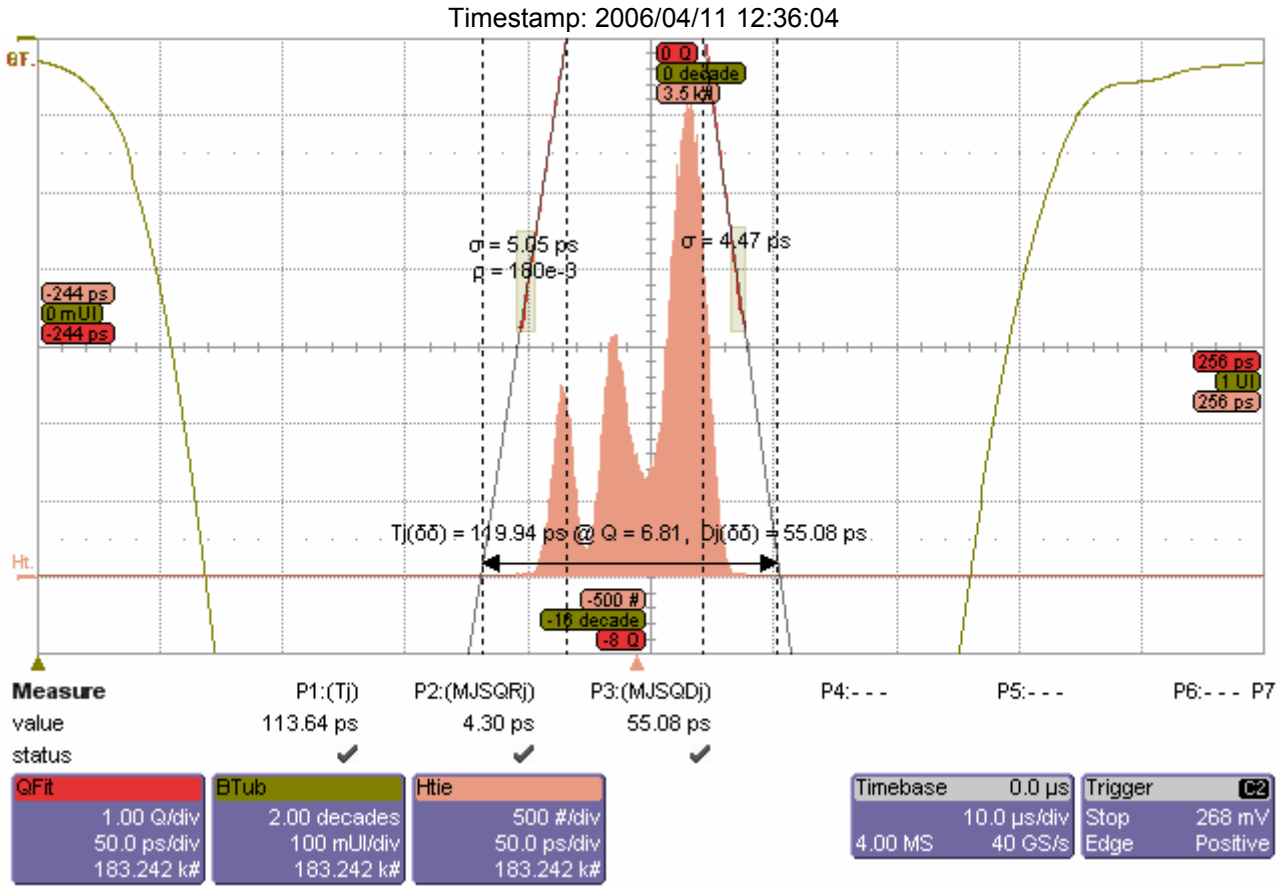
T_{TX-Dj}

TX - Deterministic Jitter

Pass

Limit Name: T_{TX-Dj}
Current Value: 0.176261032196002
Test Criteria: <=
Timestamp: 2006/04/11 12:35:44

Figure 1.1 - Reference Clock Jitter Bathtub Curve



Test 2.12 - Maximum peak-to-peak differential voltage in EI condition

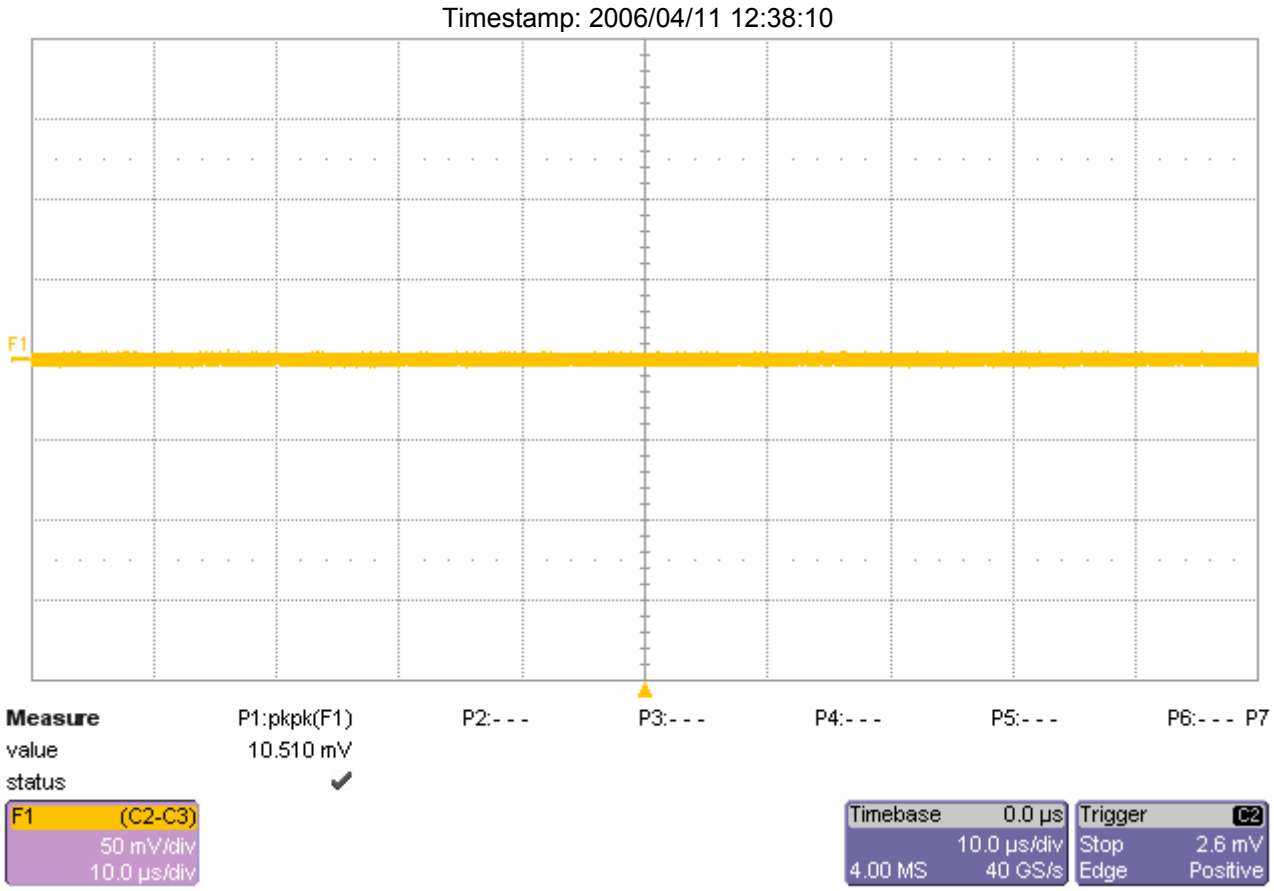
$V_{TX-IDLE-DIFFp-p}$

Maximum peak-to-peak differential voltage in EI condition

Pass

Limit Name: $V_{TX-IDLE-DIFFp-p}$
Current Value: 10.510 mV
Test Criteria: <= 40.000 mV
Timestamp: 2006/04/11 12:37:30

Figure 2.12 - Maximum Pk-Pk Differential Voltage in EI Condition.



Test 3.4 - Single-ended voltage on D+/D-

$V_{RX-SE-min\_p}$

Minimum Single-ended voltage (w.r.t. VSS) on Data+

Pass

Limit Name: V_{RX-SE}
Current Value: -8 mV
Test Criteria: -300e-3 < n < 900e-3
Timestamp: 2006/04/11 12:43:02

$V_{RX-SE-min\_n}$

Minimum Single-ended voltage (w.r.t. VSS) on Data-

Pass

Limit Name: V_{RX-SE}
Current Value: -14 mV
Test Criteria: -300e-3 < n < 900e-3
Timestamp: 2006/04/11 12:43:03

$V_{RX-SE-max\_p}$

Maximum Single-ended voltage (w.r.t. VSS) on Data+

Pass

Limit Name: V_{RX-SE}
Current Value: 350 mV
Test Criteria: -300e-3 < n < 900e-3
Timestamp: 2006/04/11 12:43:03

$V_{RX-SE-max\_n}$

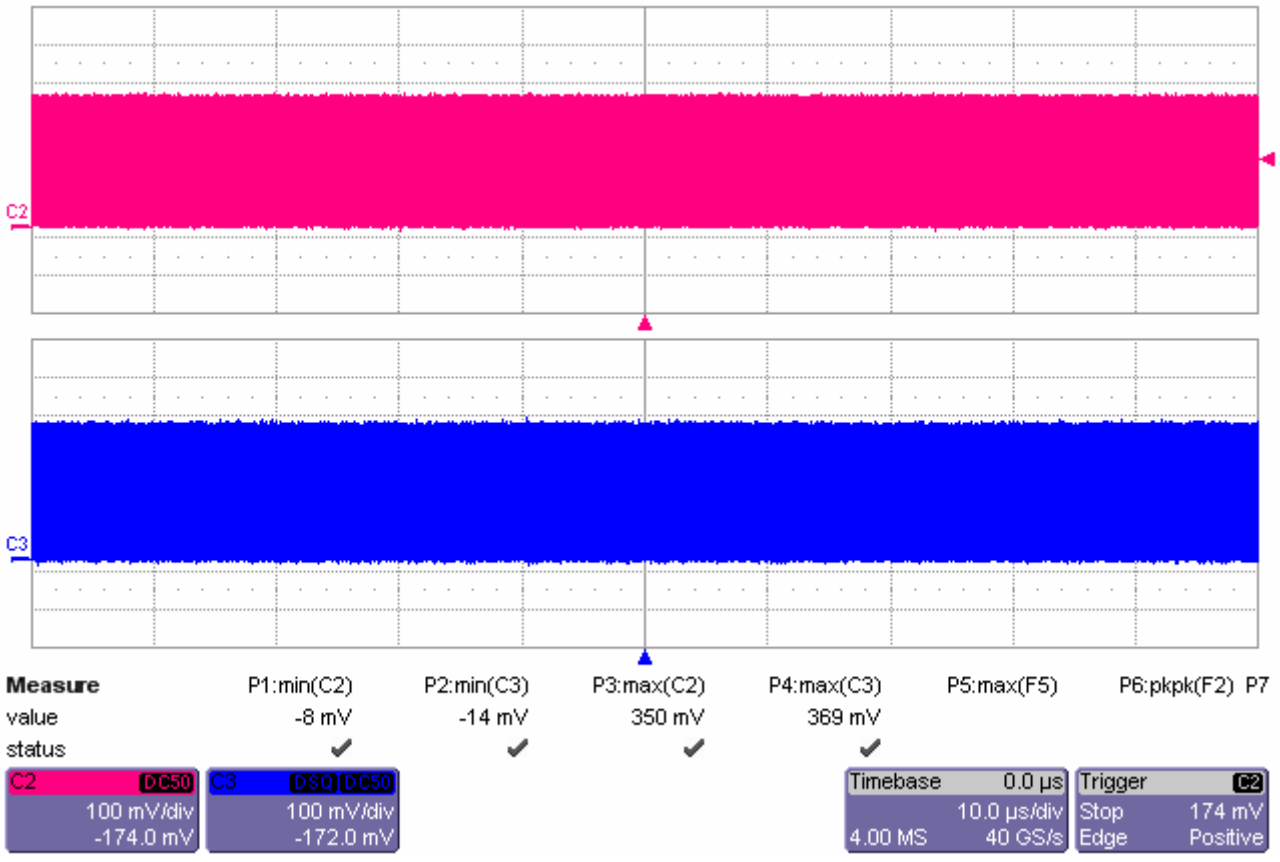
Maximum Single-ended voltage (w.r.t. VSS) on Data-

Pass

Limit Name: V_{RX-SE}
Current Value: 369 mV
Test Criteria: -300e-3 < n < 900e-3
Timestamp: 2006/04/11 12:43:04

Figure 3.4 - RX Single-Ended Voltage

Timestamp: 2006/04/11 12:43:46



Test 3.6 - Common mode of the input voltage (DC average)

V_{RX-CM}

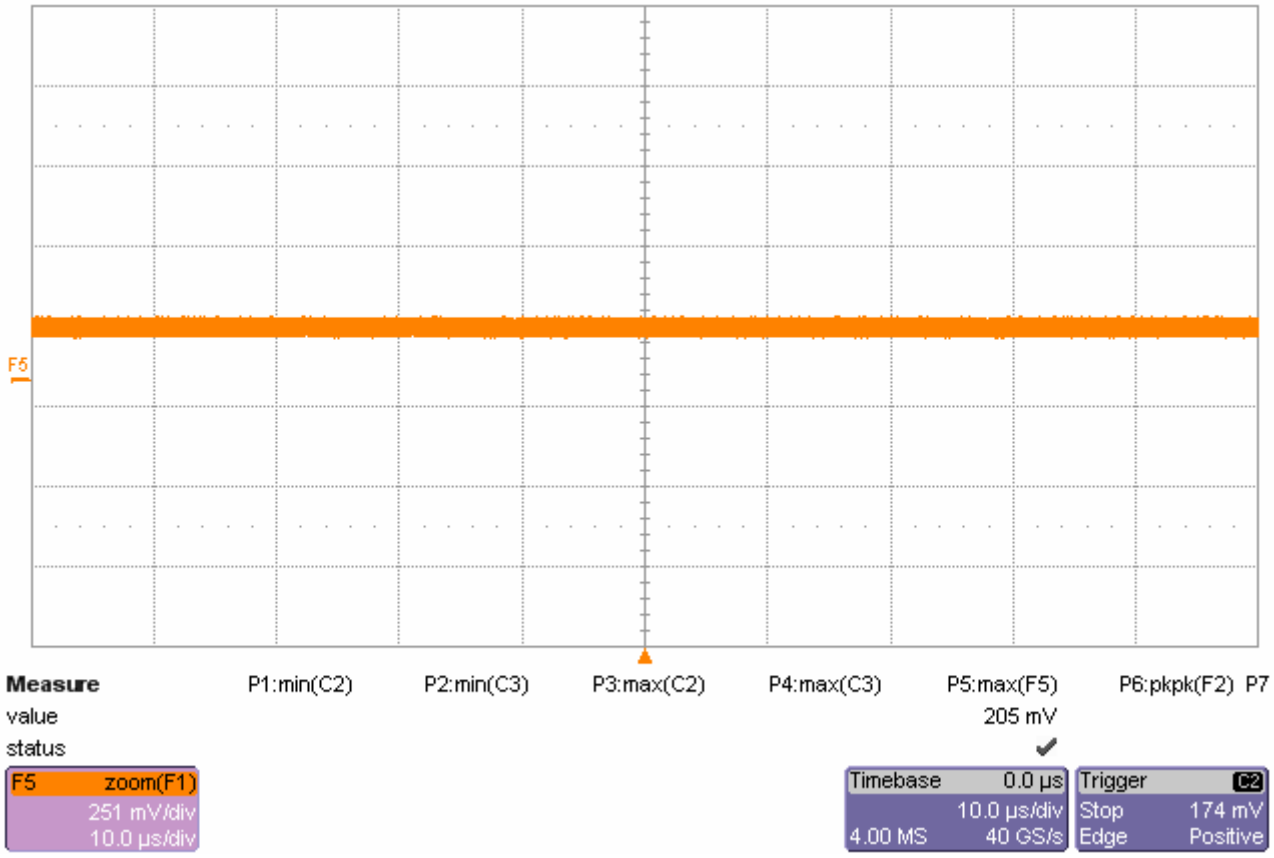
Common mode of the input voltage (DC average)

Pass

Limit Name: V_{RX-CM}
Current Value: 205 mV
Test Criteria: 120e-3 < n < 400e-3
Timestamp: 2006/04/11 12:43:57

Figure 3.6 - RX DC Common Mode Voltage.

Timestamp: 2006/04/11 12:44:48



Test 3.7 - AC peak-to-peak common mode input voltage

$V_{RX-CM-ACp-p}$

AC peak-to-peak common mode input voltage

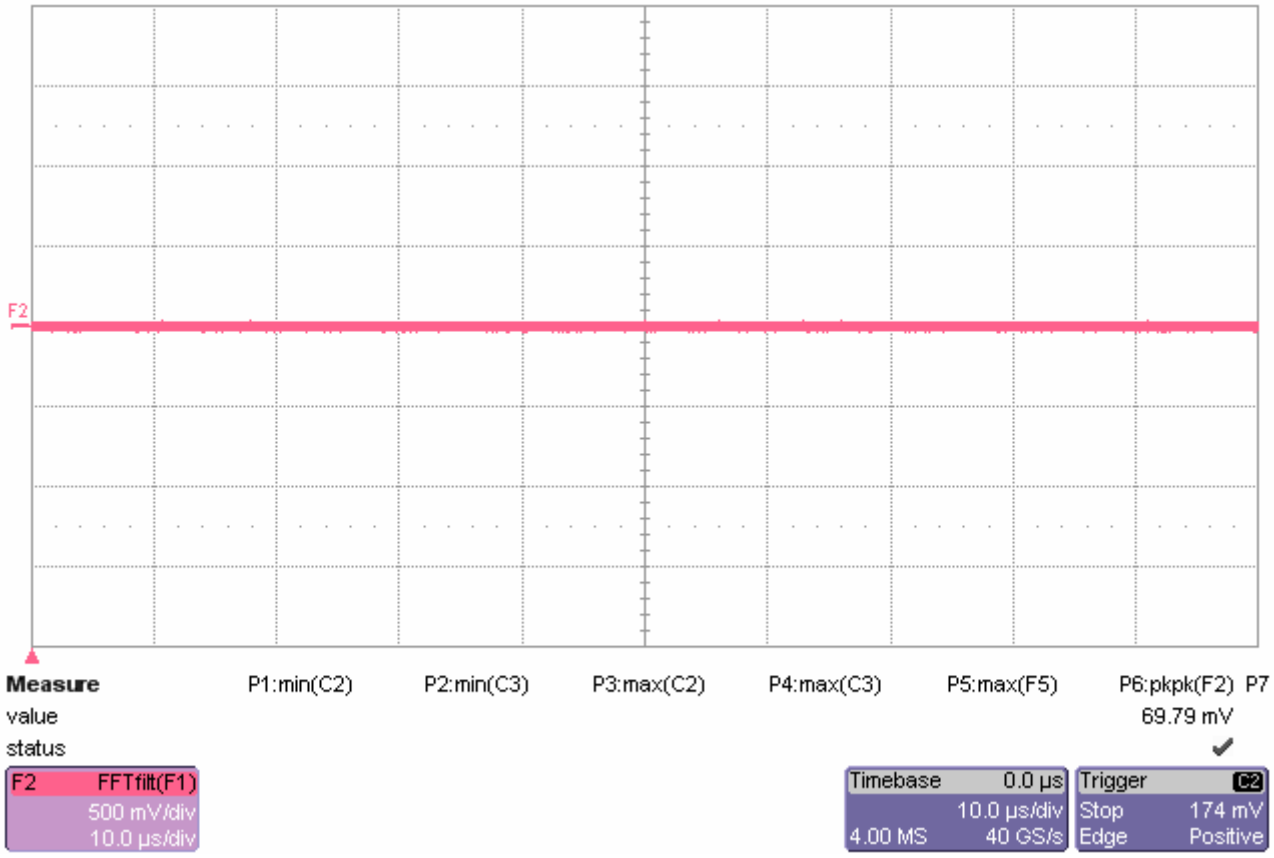
Pass

Limit Name: $V_{RX-CM-ACp-p}$
Current Value: 69.79 mV
Test Criteria: <= 270.00 mV

Timestamp: 2006/04/11 12:45:19

Figure 3.7 - RX AC Common Mode Voltage Pk-Pk

Timestamp: 2006/04/11 12:46:05



Test 3.2 - Maximum single-ended voltage in EI condition (AC + DC)

$V_{RX-IDLE-SE\_p}$

Maximum single-ended voltage in EI condition on Data+, DC + AC

Pass

Limit Name: $V_{RX-IDLE-SE}$
Current Value: 5.9 mV
Test Criteria: <= 75.0 mV
Timestamp: 2006/04/11 12:47:28

$V_{RX-IDLE-SE\_n}$

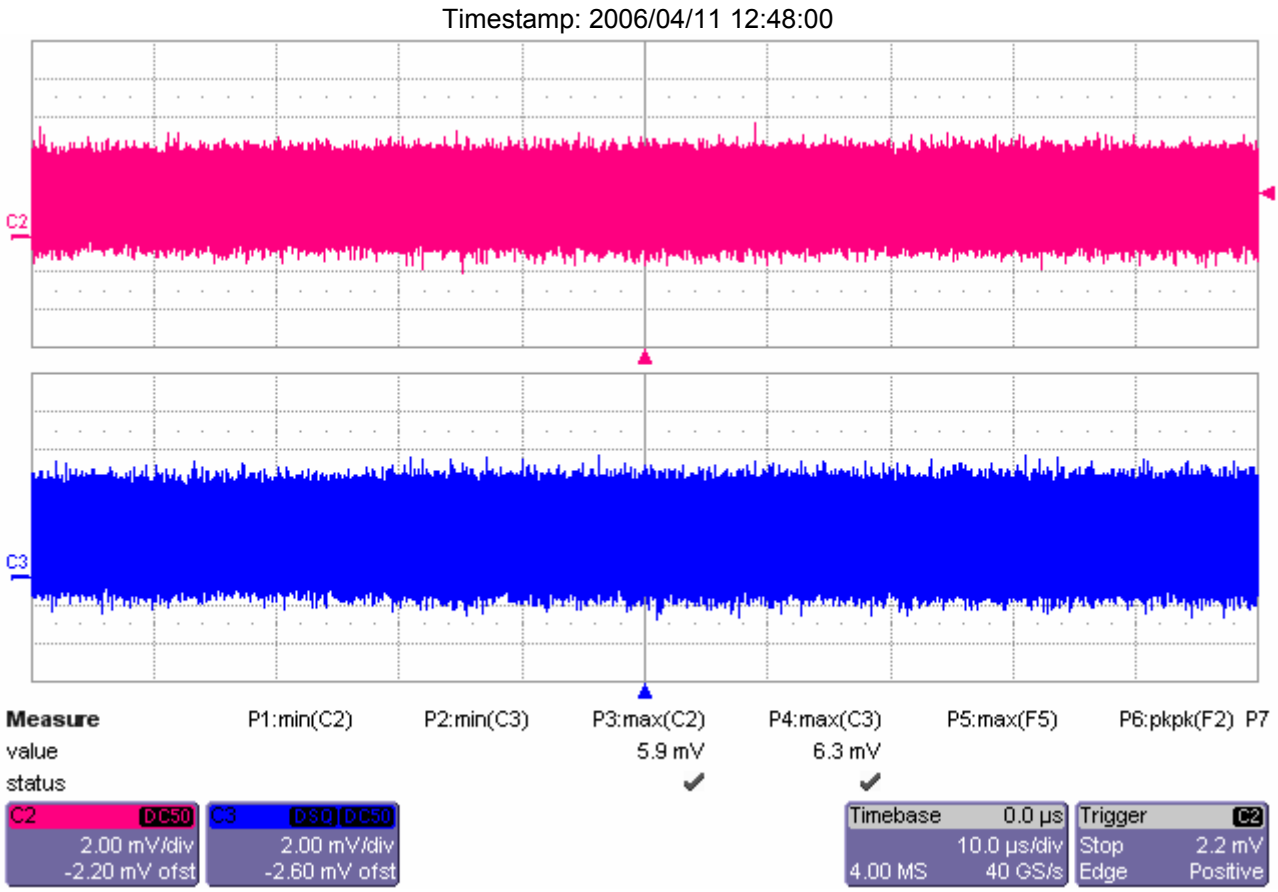
Maximum single-ended voltage in EI condition on Data-, DC + AC

Pass

Limit Name: $V_{RX-IDLE-SE}$
Current Value: 6.3 mV
Test Criteria: <= 75.0 mV

Timestamp: 2006/04/11 12:47:29

Figure 3.2 - RX Maximum Single-ended Voltage for EI Condition (AC + DC)



Test 3.1 - Differential peak-to-peak input voltage

$V_{RX-DIFFp-p-min}$

Differential peak-to-peak input voltage - minimum

Pass

Limit Name: $V_{RX-DIFFp-p-min}$
Current Value: 453 mV
Test Criteria: >= 170 mV
Timestamp: 2006/04/11 12:50:51

$V_{RX-DIFFp-p-max}$

Differential peak-to-peak input voltage - maximum

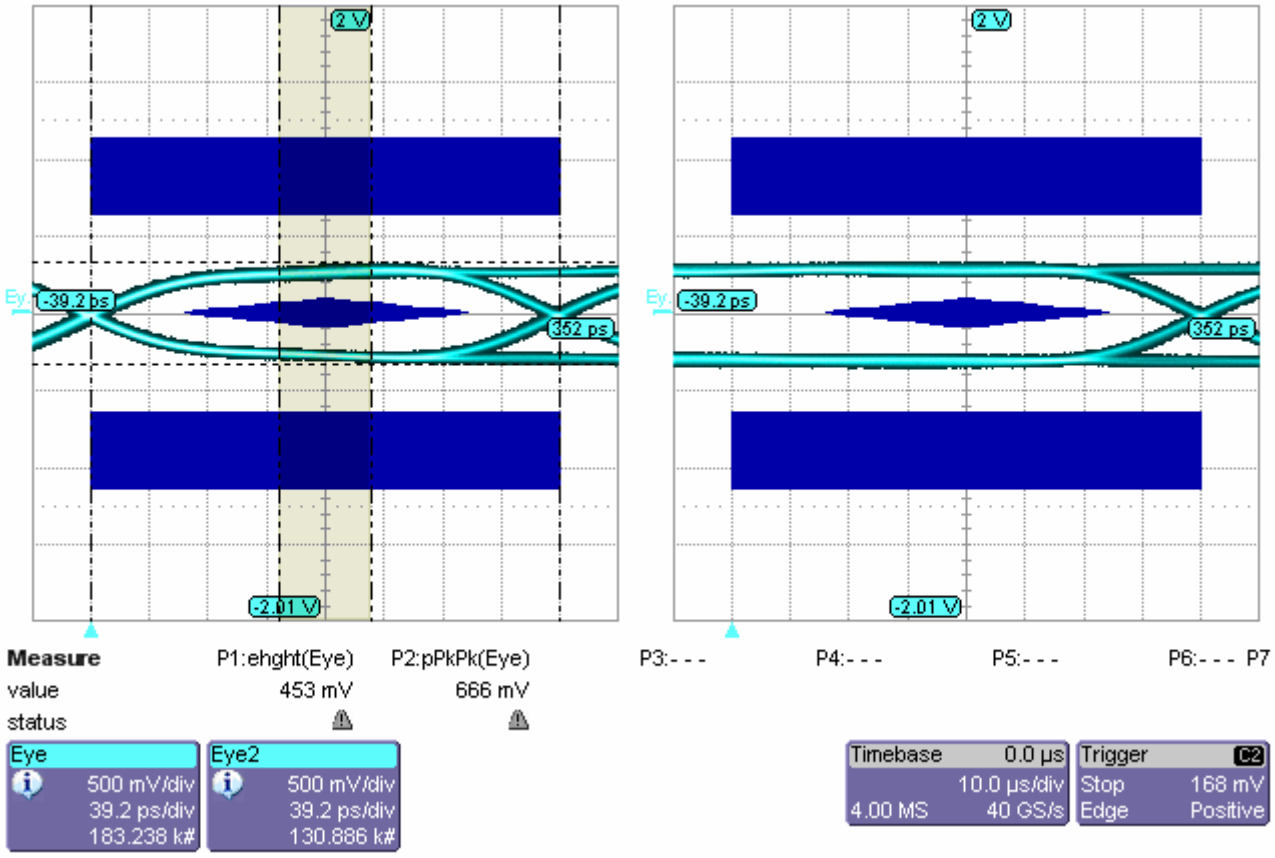
Pass

Limit Name: $V_{RX-DIFFp-p-max}$
Current Value: 666 mV
Test Criteria: <= 1.300 V

Timestamp: 2006/04/11 12:50:51

Figure 3.1 - RX Differential Pk-Pk Input Voltage.

Timestamp: 2006/04/11 12:51:30



Test 3.8 - Ratio of VRX-CM-ACp-p to minimum VRX-DIFFp-p

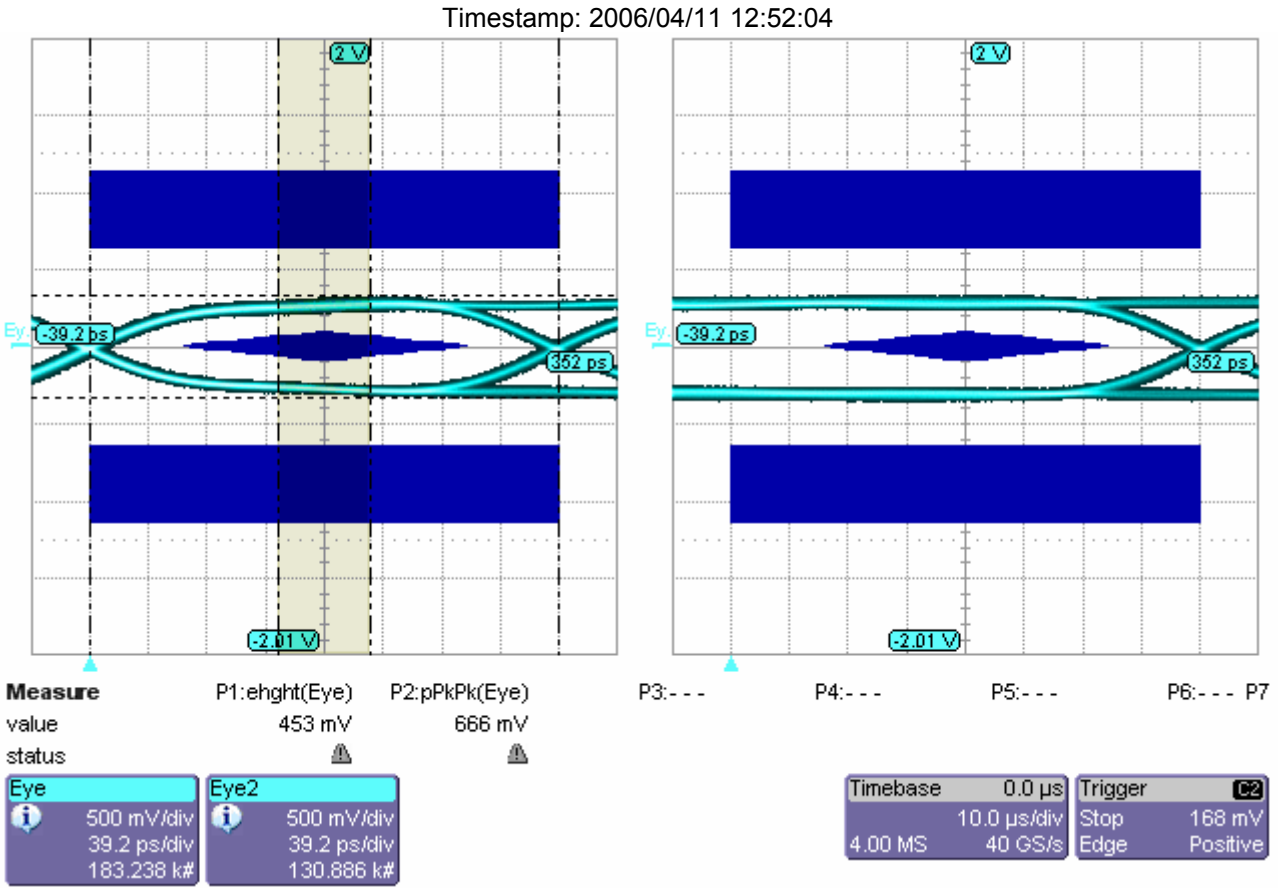
$V_{RX-CM-EH-ratio}$

Ratio of VRX-CM-ACp-p to minimum input eye height

Pass

Limit Name: $V_{RX-CM-EH-Ratio}$
Current Value: 15.4029796485509
Test Criteria: <=
Timestamp: 2006/04/11 12:51:32

Figure 3.8 - $V_{RX-CM-EH-Ratio}$ Calculation



Test 3.5.1 - Maximum RX inherent timing error

T_{RX-Tj}

Jitter Peak-to-peak

Pass

Limit Name: T_{RX-Tj}
Current Value: 0.14044373046875
Test Criteria: <=
Timestamp: 2006/04/11 12:52:35

Test 3.5.2 - Maximum RX deterministic timing error

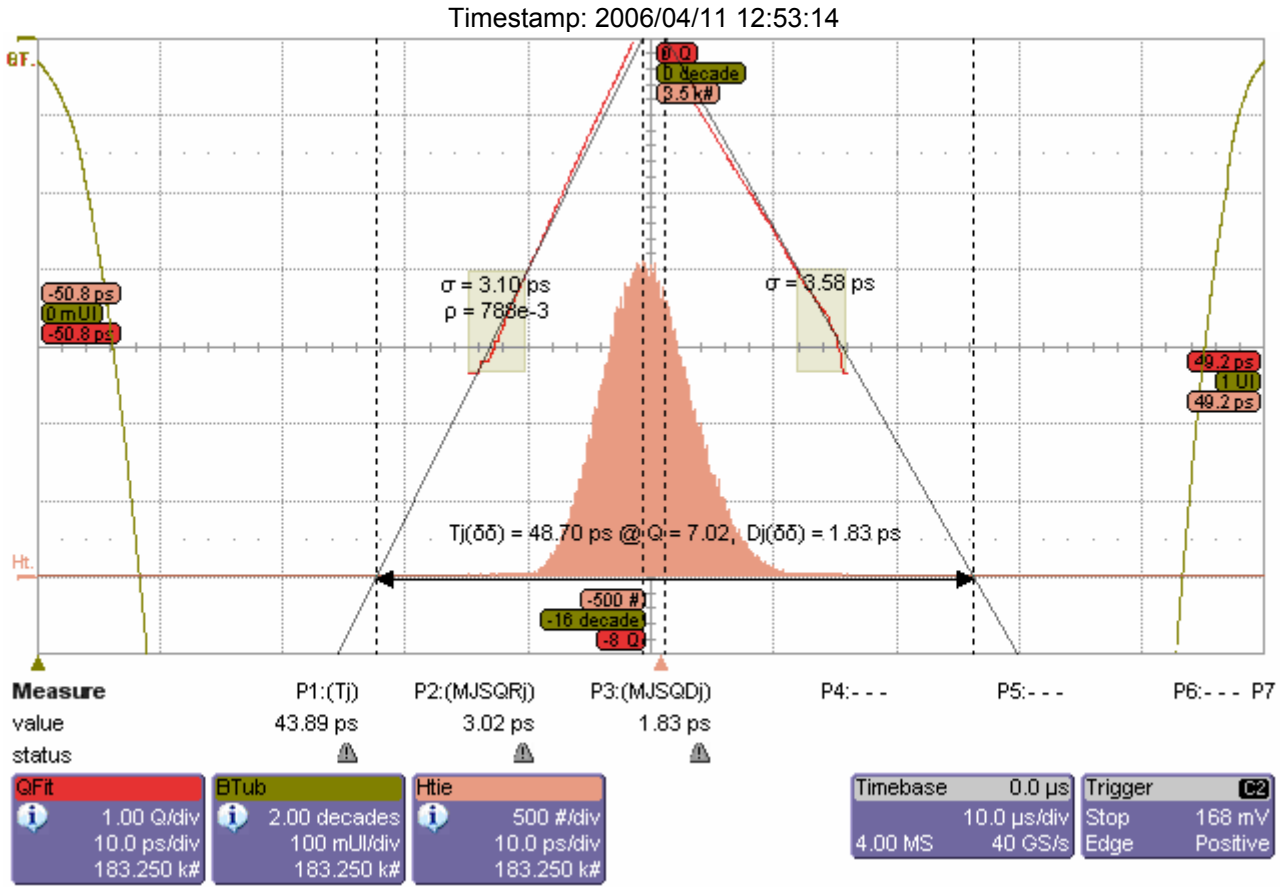
T_{RX-Dj}

RX - Deterministic Jitter

Pass

Limit Name: T_{RX-Dj}
Current Value: 5.86144647848517E-03
Test Criteria: <=
Timestamp: 2006/04/11 12:52:35

Figure 1.1 - Reference Clock Jitter Bathtub Curve



Test 3.3 - Maximum peak-to-peak differential voltage in EI condition

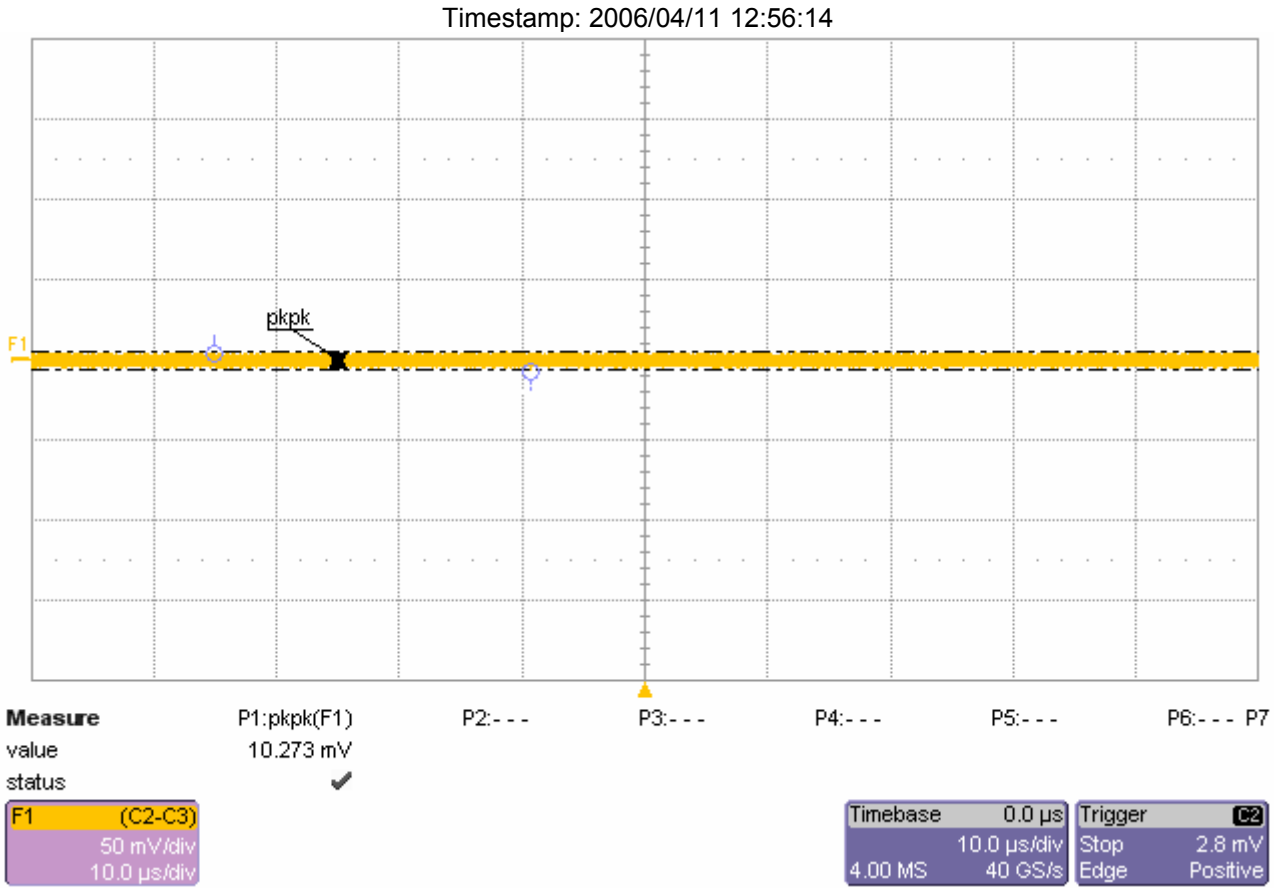
$V_{RX-IDLE-DIFF-p-p}$

Maximum peak-to-peak differential voltage in EI condition

Pass

Limit Name: $V_{RX-IDLE-DIFFp-p}$
Current Value: 10.273 mV
Test Criteria: <= 65.000 mV
Timestamp: 2006/04/11 12:55:41

Figure 3.3 - RX Maximum Pk-Pk Differential Voltage in EI Condition.



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